The Self-Describing Wishbone Bus (SDWB)

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Jule 13, 2007

About

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- VME and PCI hardware (FPGA based)
- I work on Linux device drivers

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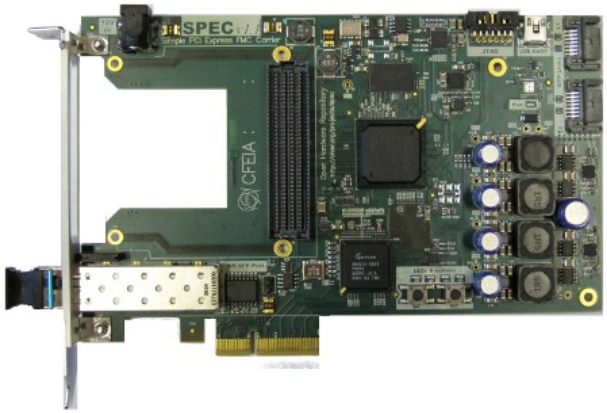
- Dynamic hardware logic!

FPGA Hardware at CERN



(a) SPEC Board

(b) White Rabbit Switch

Figure: Open Hardware from OHWR

Wishbone Bus

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- Integrator places logic blocks in Wishbone address space
- Mapped and accessed as usual

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- Clean design: Bus auto-discovery
  - Not defined in the Wishbone specification
  - Let's add one!

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- Should not force the use of external sources for metadata

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- Only header block location needed

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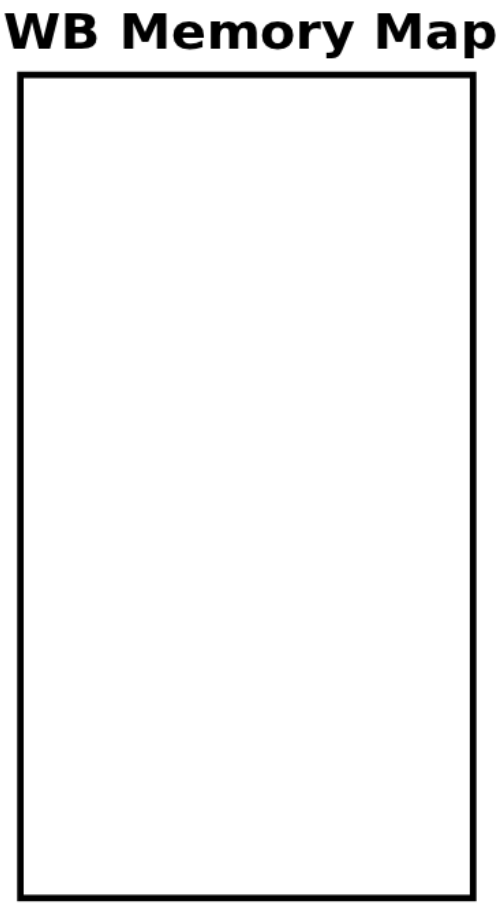
  - Relative offsets
- Array of top level devices. Location in header

Auto-discovery!



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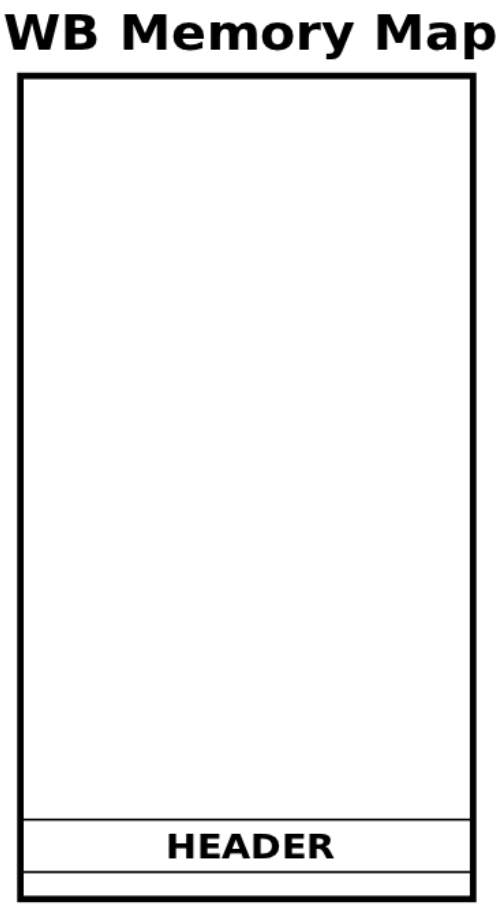

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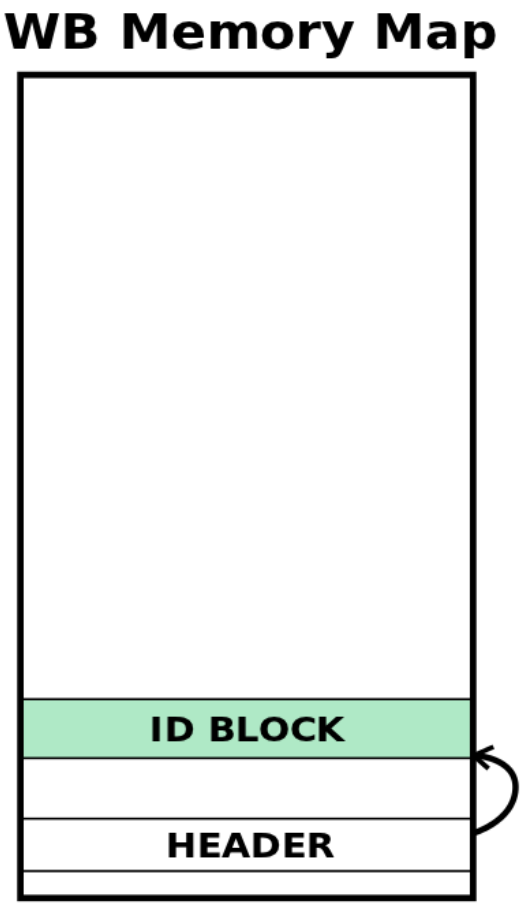

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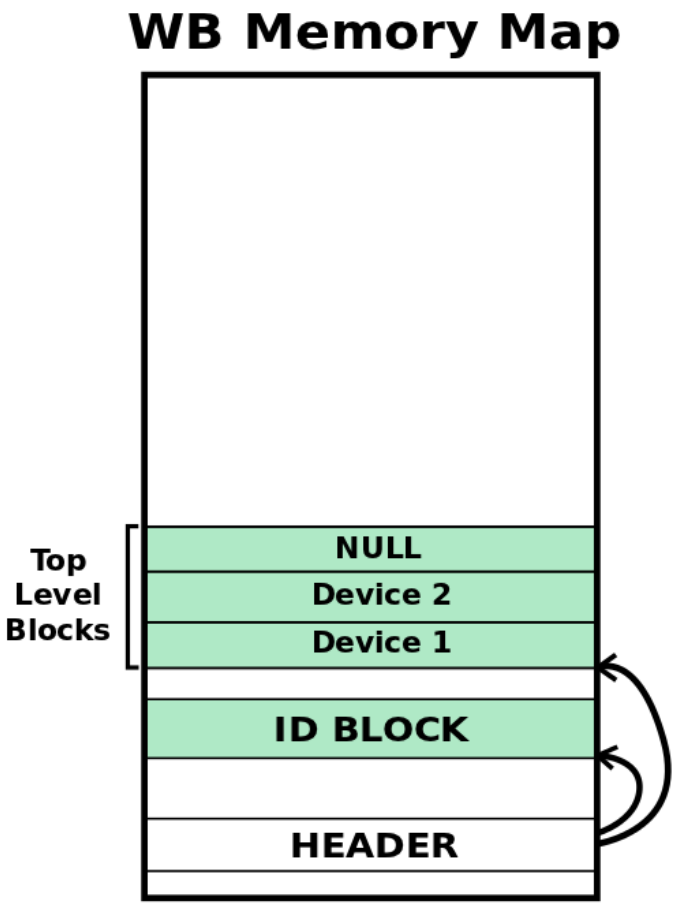

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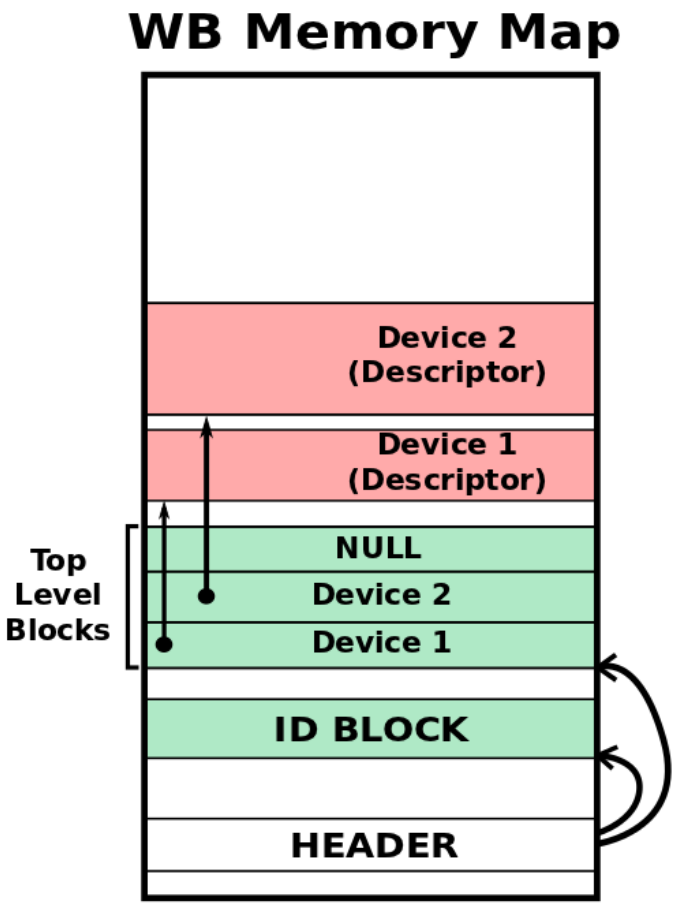

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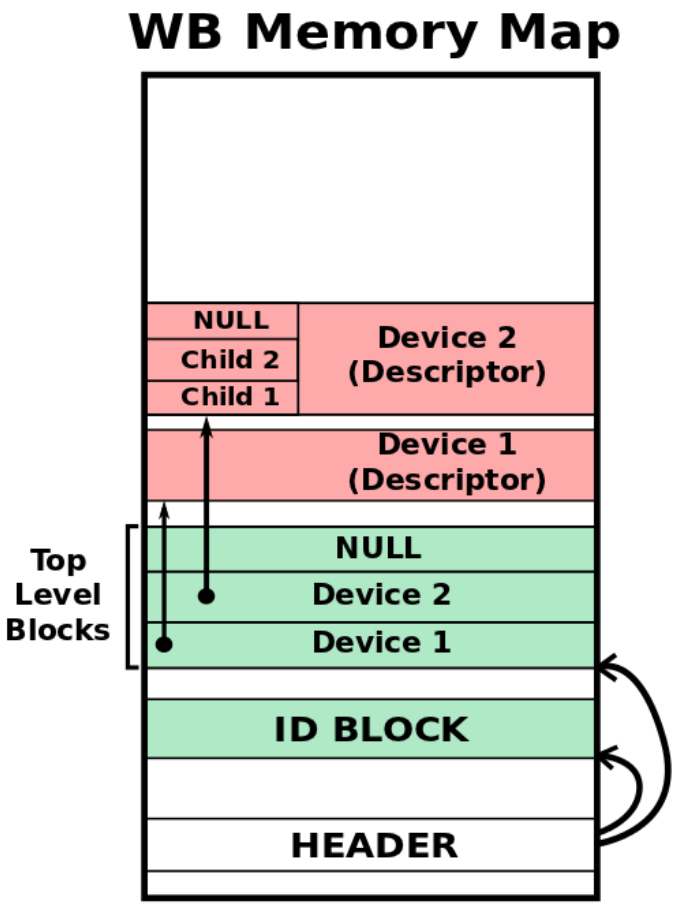

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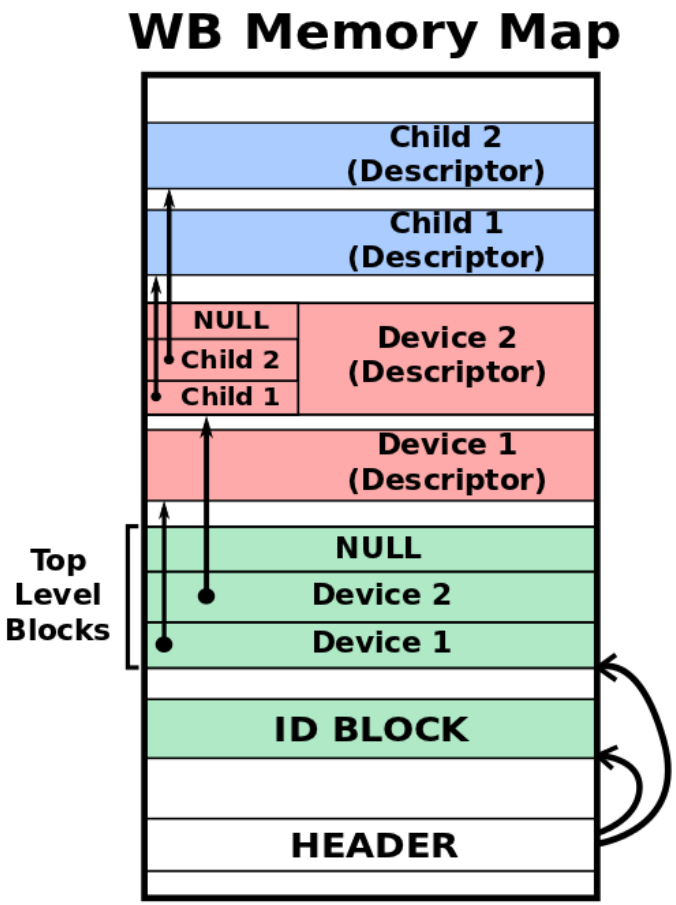

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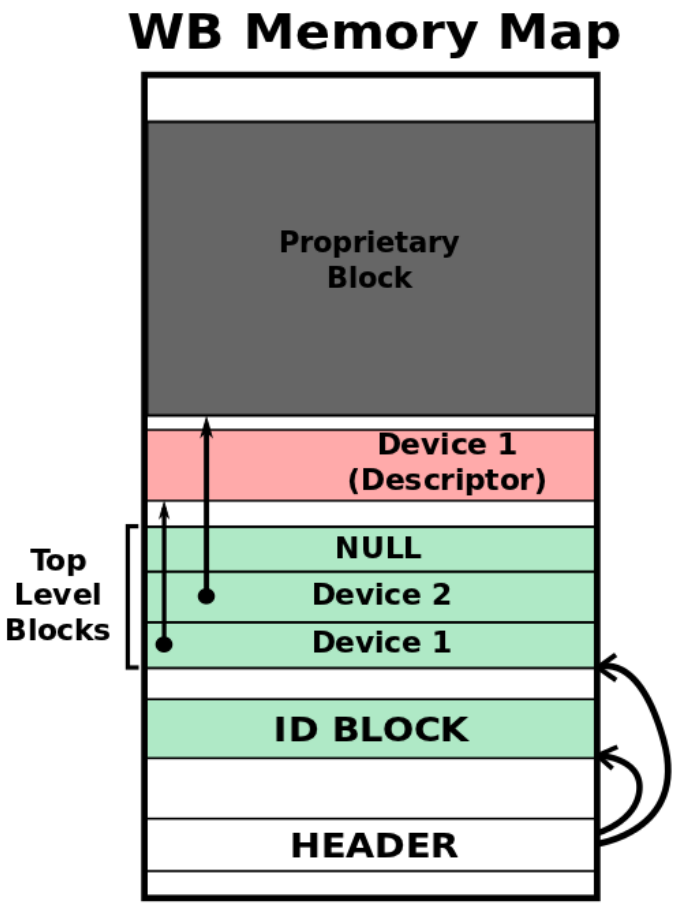

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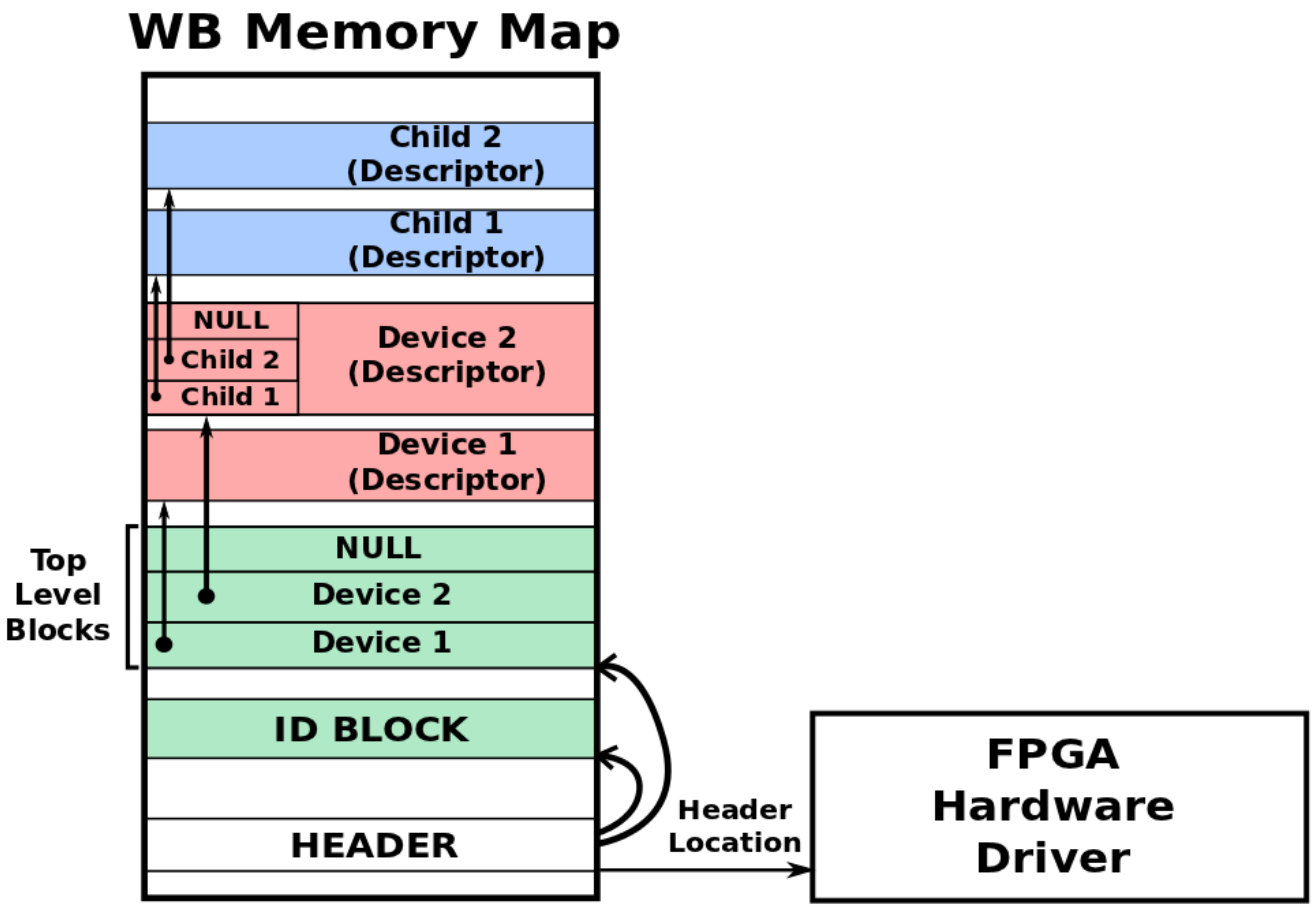

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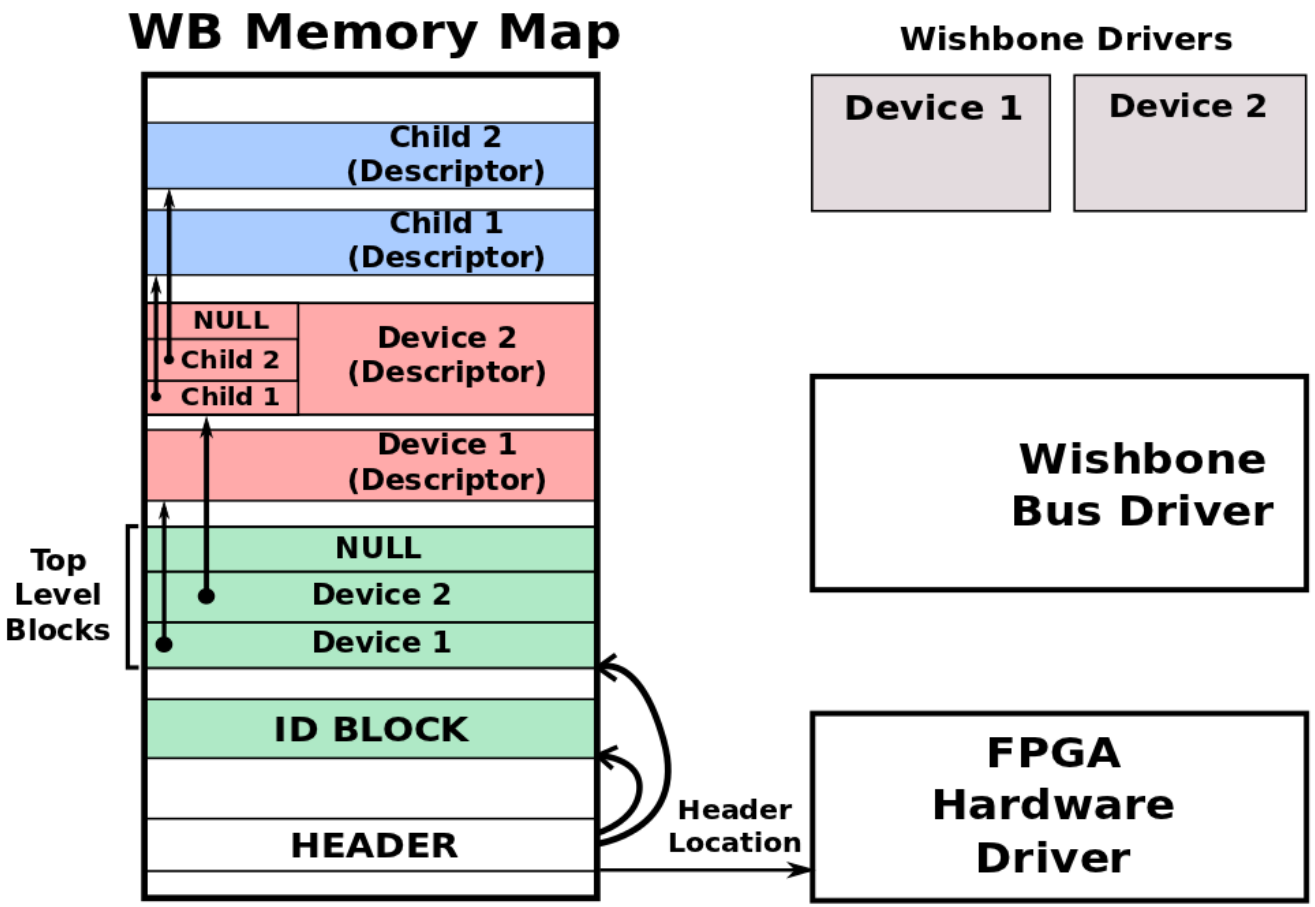

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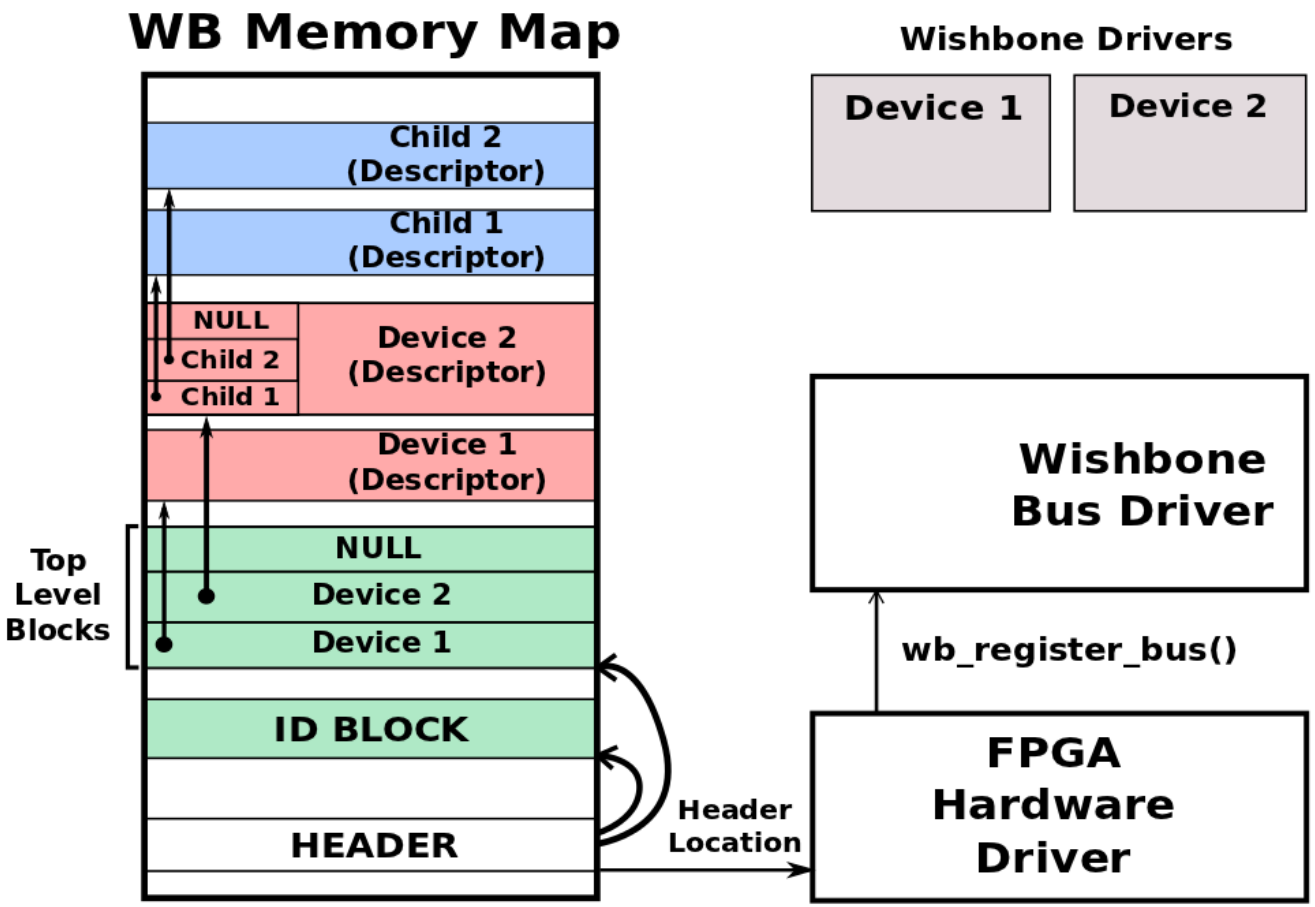

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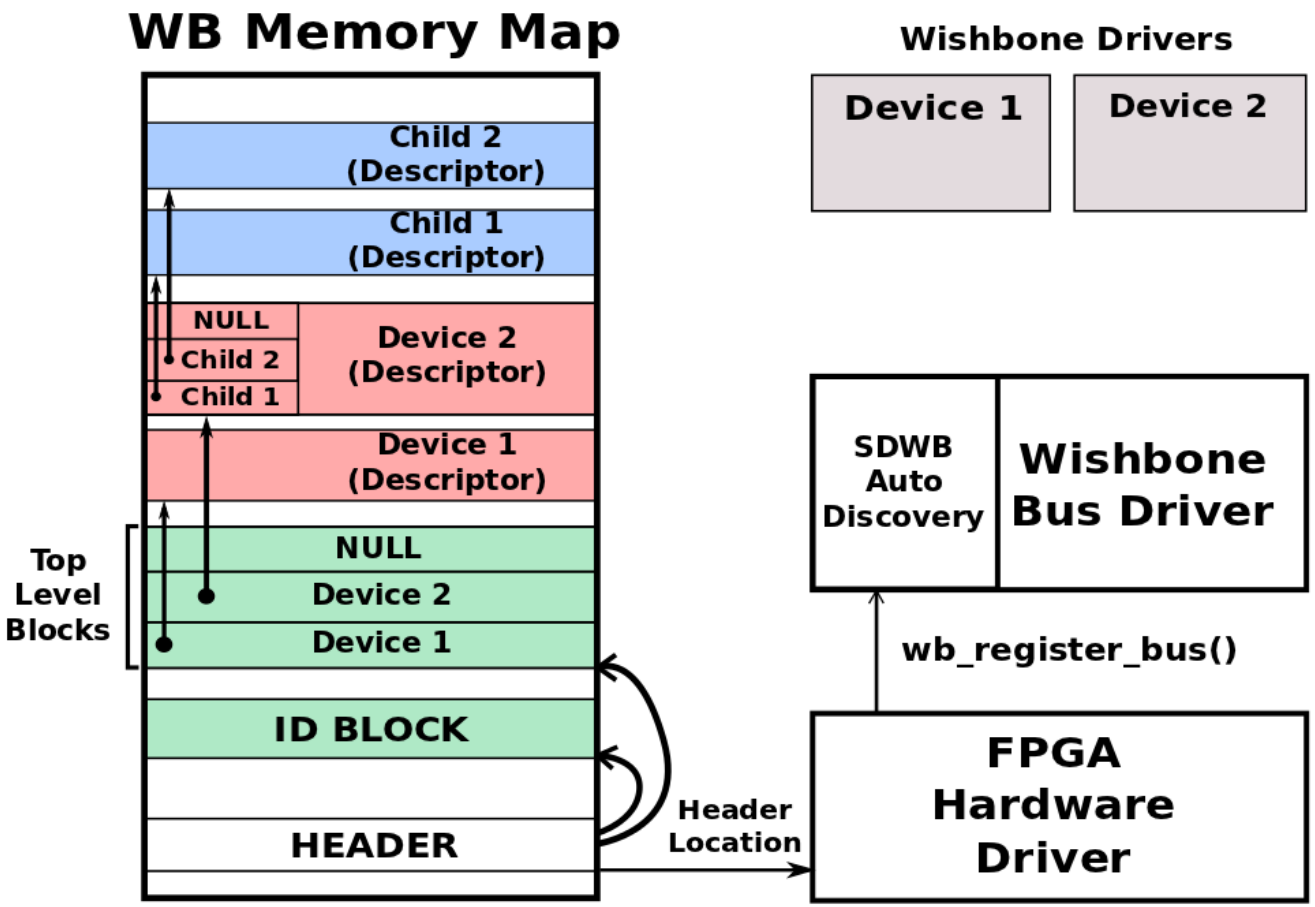

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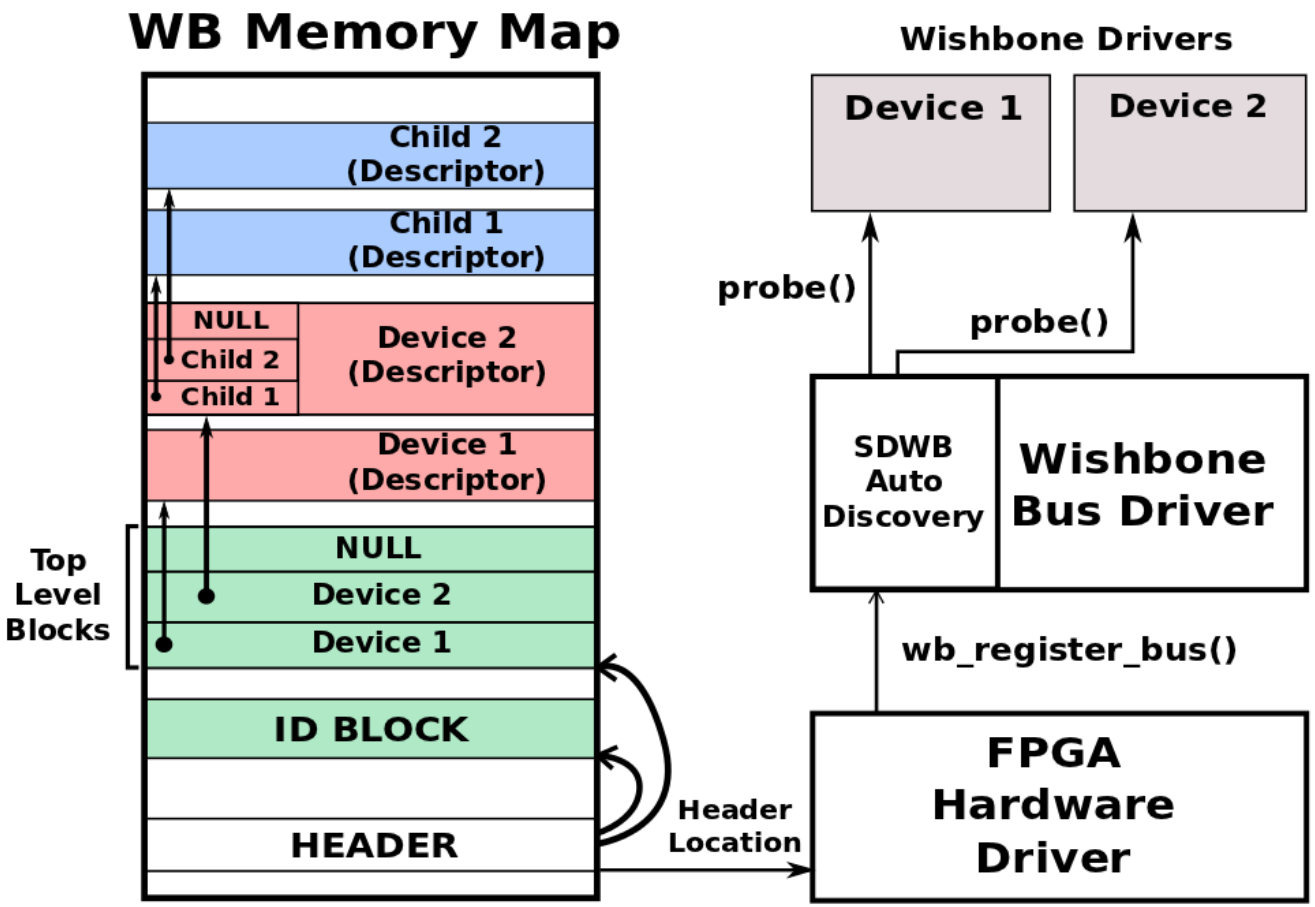

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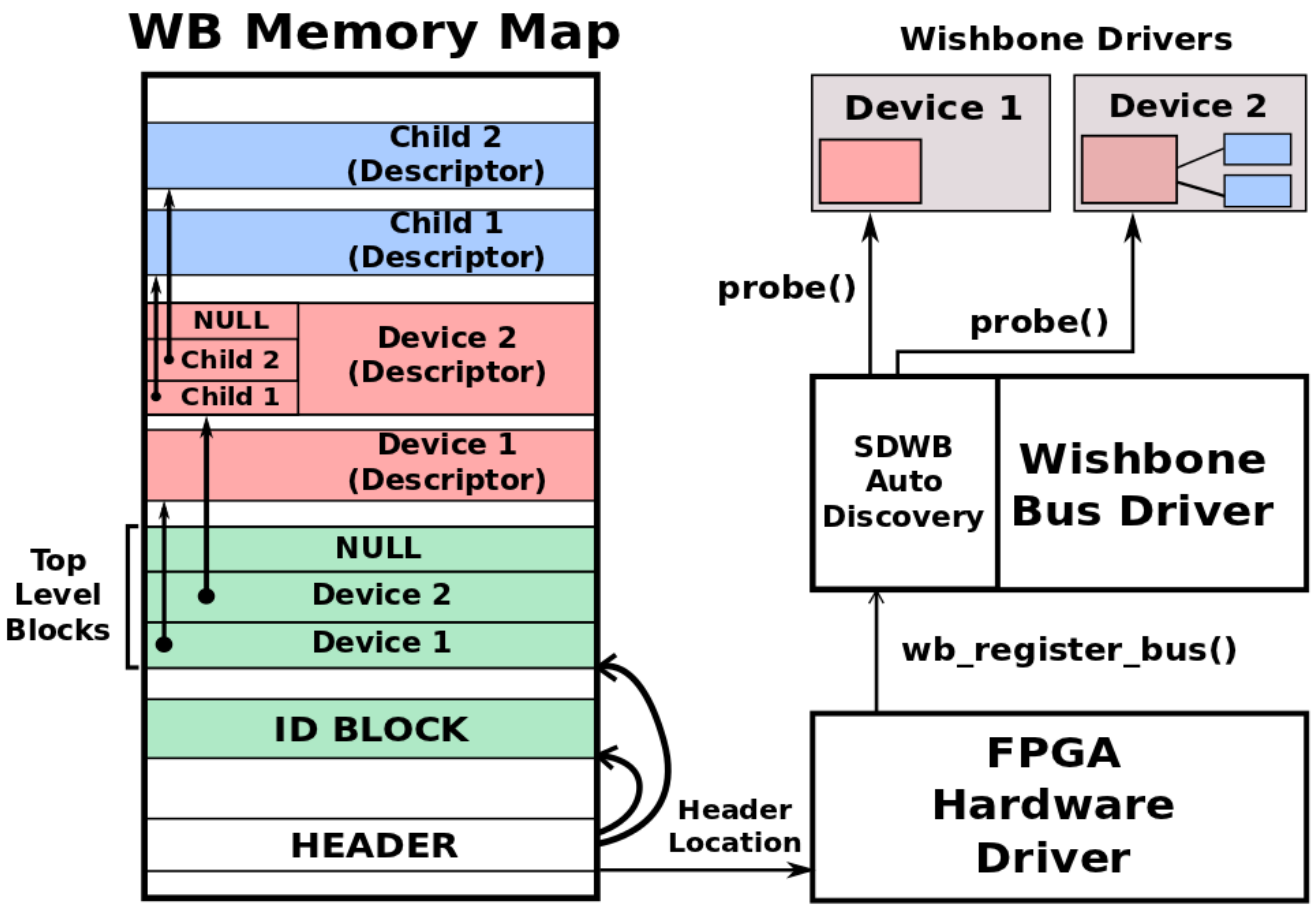

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  - Drivers for specific blocks

Thanks!

- OHWR Page:
  http://www.ohwr.org/projects/fpga-config-space