Who Ate My Battery?

Why Free and Open Source Systems Are Solving the Problem of Excessive Energy Consumption

Jeremy Bennett, Embecosm Kerstin Eder, Computer Science, University of Bristol





Why?



Ericsson T65

- released 2001
- Li-Ion 720 mAh
- standby 300 h
- talk time 11 h
- includes talk/standby prediction



Sony Ericsson Xperia X10 mini

- released 2010
- Li-polymer 930 mAh
- standby up to 285 h (3G) / 360 h (2G)
- talk time up to 4 h (2G) / 3.5 h (3G)







All Computers Large and Small

















Some Mathematics

Energy = Power x Time

or

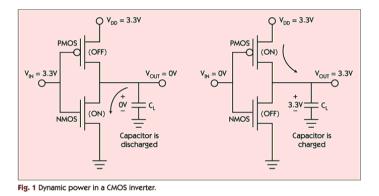
Power = *Energy* ÷ *Time*

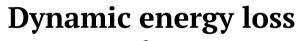




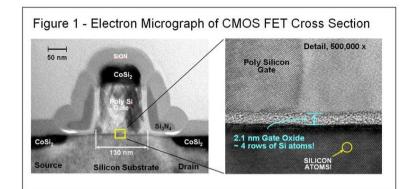


Hardware Engineers are Very Good Dynamic Voltage and Frequency Scaling





$P \propto$	$V^2 R$	f	\sim	V	
$P \propto$	f^3				
E =	P.t	and	t	=	1/f
$E \propto$	f^2	and	E	\propto	V^2



Static energy loss $P = V^2 R$ and $f \propto V$ $P \propto f^2$ E = P t and t = 1/f $E \propto f$ and $E \propto V$

Turn off circuits that are not being used: clock gating

Atmel AVR ATxmega256 @3.0V and 2MHz:Idle current 290μAAtmel AVR ATxmega256 @1.8V and 32kHz:Idle current4μA







Energy Transparency from Hardware to Software

Kerstin Eder **Design Automation and Verification, Microelectronics**











Free Mobile Apps "Drain Battery Faster"



Free mobile apps 'drain battery faster'

Free mobile apps which use third-party services to display advertising consume considerably more battery life, a new study suggests.

Researchers used a special tool to monitor energy use by several apps on Android and Windows Mobile handsets.

Findings suggested that in one case 75% of an app's energy consumption was spent on powering advertisements.



Like many games, Angry Birds has a free version supported by targeted advertising

Report author Abhinav Pathak said app makers must take energy optimisation more seriously.

Related Stories









Energy-Aware System Design

 Power management largely in domain of Hardware Design

- Considerations to minimize/optimize
 - Dynamic (switching) and static (leakage) power
 - Energy consumption
- On-chip power management
 - DVFS
 - Modes: on, standby, suspend, sleep, off
- Where can the greatest savings be made?

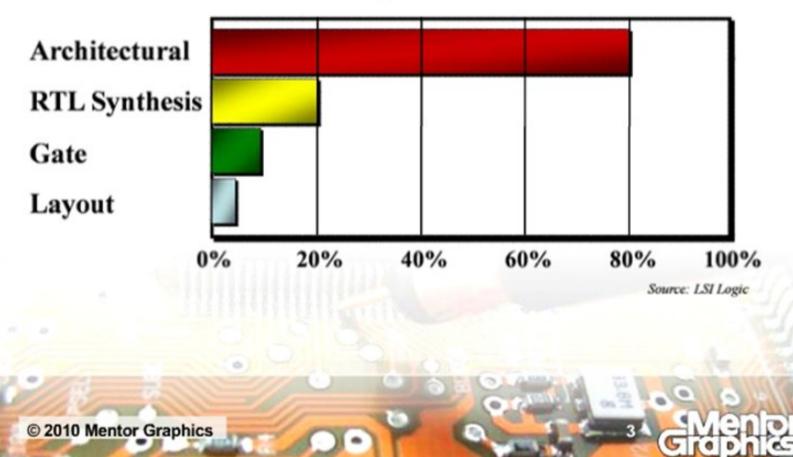






Greater Savings at Higher Levels

Why Optimize Power at the Architecture?



Power Optimization Potential







news

LOW POWER

Lack of software support marks the low power scorecard at DAC

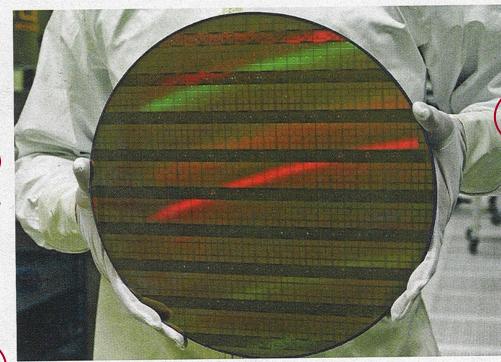
ne of the panels at the Design Automation Conference (DAC), which took place in California in early June, set out to get an idea of how well the industry is doing at delivering lower-power systems.

It is becoming clear, writes Chris Edwards, that the system level is currently the missing link.

Processes can deliver some gains – and Globalfoundries' Andrew Brotman was able to outline some of the features that the foundry has put into its recently launched low-power high-k, metal gate (HKMG) process.

FinFETs should bring power down as those processes become available, although they are not the only eptions. But if the software keeps cores active for no good reason, the lower switching power per bit processed won't deliver a realised saving.

In his keynote speech Gadi Singer, vice-president IAG and general man ager of the SoC enabling group at Intel Corporation, said that with limited software support, dedicated low-



Intel waits for better low-power software control

power circuitry could save maybe 20% in a typical multimediaoriented core.

Make the software controlling it

better at controlling the power states and that difference could be three to five times.

During an afternoon panel discus-

sion Ambrose Low, director of design engineering at Broadcom said: "We have hundreds of knobs in the hardware to turn power down.

"The question is whether we can take the actual use-cases into consideration and optimise the software to power the logic circuits down. We still have a long way to go."

Ruggero Castagnetti of LSI argued that the desire to do more in software will grow.

"As we see power limits and targets becoming unachievable, customers will be willing to go to that extra step. There is a challenge that needs to be addressed and we have to do more on the systems side," Castagnetti satd.

"We should put a challenge to the software designers to see how much power they can save," he added.

Chris Edwards writes the Low-Power Design Blog (enabled by Mentor Graphics) on ElectronicsWeekly.com

www.electronicsweekly.com/ew-blogs/



Wasted Potential

Huge advances have been made in power-efficient hardware.

Various software-controllable energy-saving features available, such as DVFS, power modes.

BUT – potential energy savings are wasted by

- software that does not exploit energy-saving features of hardware;
- poor dynamic management of tasks and resources.









The Focus is on Software

- Software controls the behaviour of the hardware
 - Algorithms and Data Flow
 - Compiler (optimizations)
 - traditional SW design goals:
 - performance, performance, performance
- Software engineers often "blissfully unaware"
 - Implications of algorithm/code/data on power/energy?
 - Power/Energy considerations
 - at best, secondary design goals
 - BUT the biggest savings can be gained from optimizations at the higher levels of abstraction in the system stack – this includes Algorithms, Data and SW







Aligning SW Design Decisions with Energy-Efficiency Design Goal

Key steps*:

- "Choose the best algorithm for the problem at hand and make sure it fits well with the computational hardware. Failure to do this can lead to costs far exceeding the benefit of more localized power optimizations.
- Minimize memory size and expensive memory accesses through algorithm transformations, efficient mapping of data into memory, and optimal use of memory bandwidth, registers and cache.
- Optimize the performance of the application, making maximum use of available parallelism.
- Take advantage of hardware support for power management.
- Finally, select instructions, sequence them, and order operations in a way that minimizes switching in the CPU and datapath."
- Kaushik Roy and Mark C. Johnson. 1997. "Software design for low power". In *Low power design in deep submicron electronics*, Wolfgang Nebel and Jean Mermet (Eds.). Kluwer Nato Advanced Science Institutes Series, Vol. 337. Kluwer Academic Publishers, Norwell, MA, USA, pp 433-460.







6.3. SOFTWARE DESIGN FOR LOW POWER

KAUSHIK ROY AND MARK C. JOHNSON School of Electrical and Computer Engineering Purdue University West Lafayette, Indiana, U.S.A.

1. Introduction

It is tempting to suppose that only hardware dissipates power, not software. However, that would be analogous to postulating that only automobiles burn gasoline, not people. In microprocessor, micro-controller, and digital signal processor based systems, it is software that directs much of the activity of the hardware. Consequently, the software can have a substantial impact on the power dissipation of a system. Until recently, there were no efficient and accurate methods to estimate the overall effect of a software design on power dissipation. Without a power estimator there was no way to reliably optimize software to minimize power. Since 1993, a few researchers have begun to crack this problem. In this chapter, you will learn

Energy Transparency

Information on energy usage is available for programs:

- (ideally) without executing them, and
- at all levels from machine code to high-level application code.







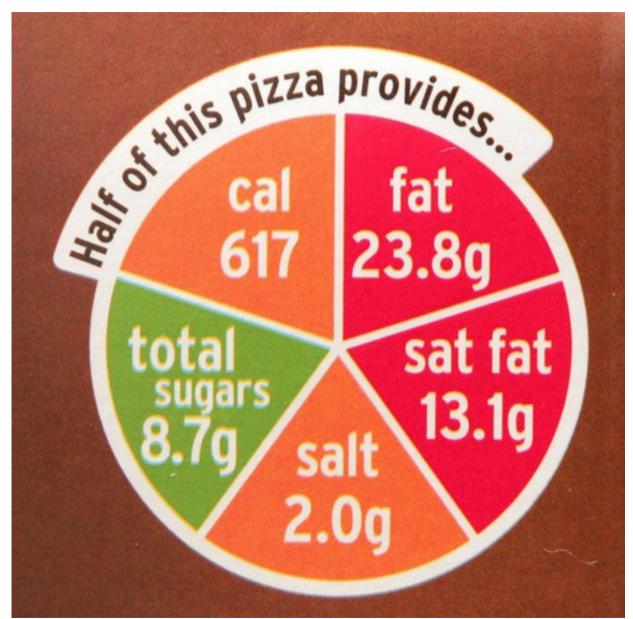








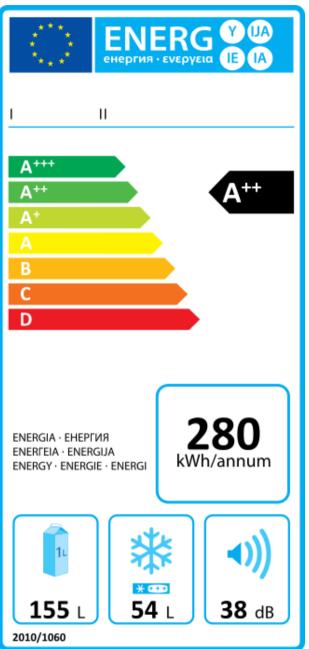
Transparency











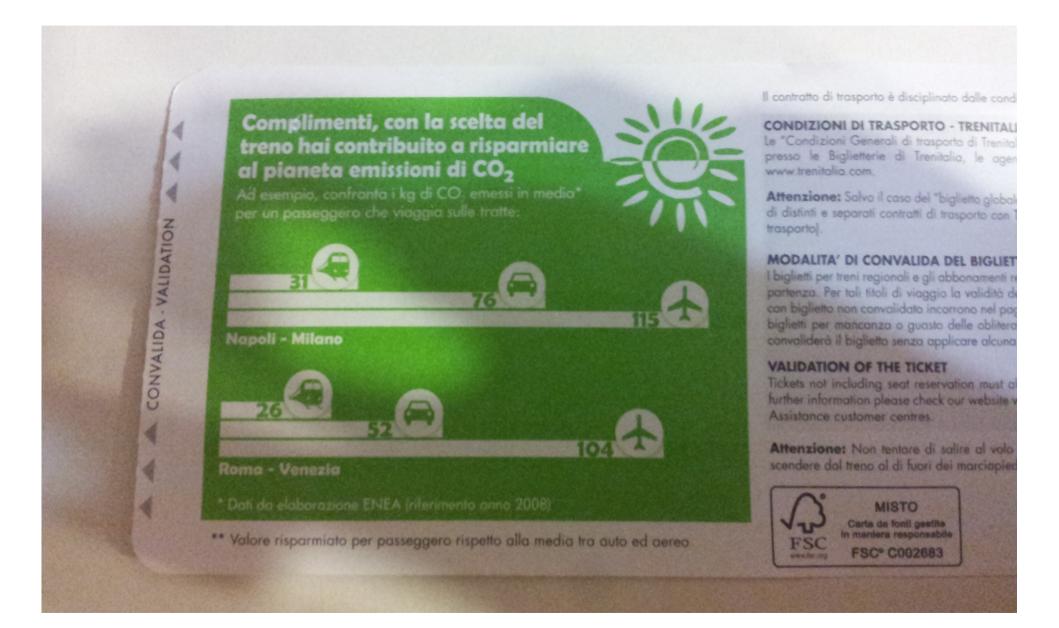
Transparency







Transparency











Why Energy Transparency?

Energy transparency enables a deeper understanding of how algorithms and coding impact on the energy consumption of a computation when executed on hardware.







The EACOF

A simple <u>Energy-Aware</u> <u>Computing</u> <u>Framework</u>

https://github.com/eacof/eacof







Comparing Sorting Algorithms

Data Type uint8_t uint16 t uint32_t uint64_t Total Average Total Average Total Average Total Total Total Total Total Time Energy Power Time Energy Power Time Energy Power Time Energy Algorithm (J) (W) (W) (J) (W) Num Elements (s) (s) (J) (s) (J) (s)Bubble Sort 50,000 5.5312.035.3912.095.665.7866.66 65.2969.0512.1971.83**1**02.18 12.757.98 13.21 Insertion Sort 200,000 7.98 $\blacksquare 103.00$ 12.857.4698.81 7.54 $\blacksquare 105.03$ Quicksort 2,000,000 5.5161.7311.205.5361.9011.195.5261.6011.155.5162.90•6.06 72.33 12.3660,000,000 11.936.07 72.4611.936.1275.655.93 76.98 Merge Sort 72.39 12.376.7986.29 12.69●73.25 100,000,000 •5.84 6.1576.9012.48•5.69 qsort 12.75Counting Sort 200,000,000 0.240.23♦2.92 ♦3.16 13.230.25♦3.58 14.150.35♦5.12

Sorting of integers in [0,255]

- Insertion Sort: 32 bit version more optimized
- Counting Sort:

75% more energy for 64 bit compared to 8 bit values

- Sorting 64 bit values takes less time than sorting 8 bit values, but consumed more energy
- ★ Average power variations between algorithms

Hayden Field, Glen Anderson, Kerstin Eder, EACOF: A Framework for Providing Energy Transparency to enable Energy-Aware Software Development. *29th ACM Symposium On Applied Computing*. pp. tbc-tbc. March 2014.





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Average

Power

(W)

12.41

13.89

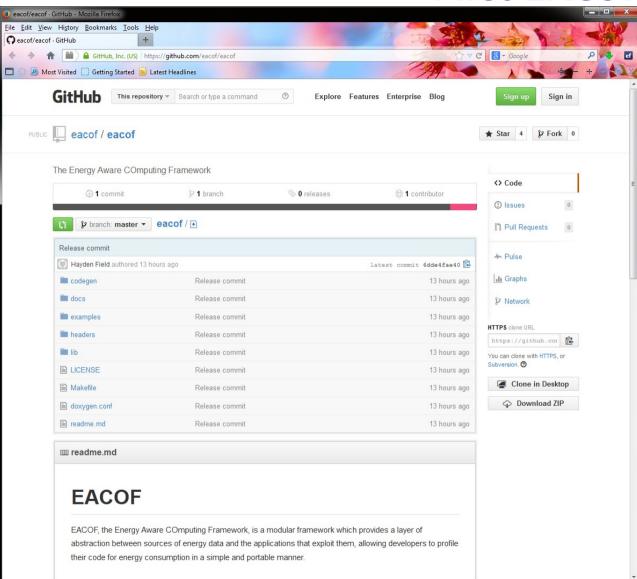
12.86

14.44

★11.42

★12.98

First EACOF release



https://github.com/eacof/eacof

















The ENTRA Project

- Whole Systems ENergy TRAnsparency
 - 1.10.2012 30.9.2015
 - EC FP7 FET MINECC:

"Software models and programming methodologies supporting the strive for the energetic limit (e.g. energy cost awareness or exploiting the trade-off between energy and performance/precision)."













Energy Modelling

Data to enable Energy Transparency





Energy Modeling

Energy Cost (E) of a program (P):

$$E_{P} = \sum_{i} (B_{i} \times N_{i}) + \sum_{i,j} (O_{i,j} \times N_{i,j}) + \sum_{k} E_{k}$$

Instruction
Base Cost,
 B_{i} , of each
instruction i
Circuit State
Overhead, $O_{i,j}$,
for each
instruction pair
Other
Instruction
Effects
(stalls, cache
misses, etc)

V. Tiwari, S. Malik and A. Wolfe. "Instruction Level Power Analysis and Optimization of Software", Journal of VLSI Signal Processing Systems, 13, pp 223-238, 1996.







XCore Energy Modelling

Energy Cost (E) of a multi-threaded program (P):

$$E_{p} = P_{base}N_{idle}T_{clk} + \sum_{t=1}^{N_{t}}\sum_{i\in ISA} \left(\left(M_{t}P_{i}O + P_{base}\right)N_{i,t}T_{clk} \right) \right)$$

Idle base power and duration Concurrency cost, instruction cost, generalised overhead, base power and duration

- Use of execution statistics rather than execution trace.
- Fast running model with an average error margin of less than 7%

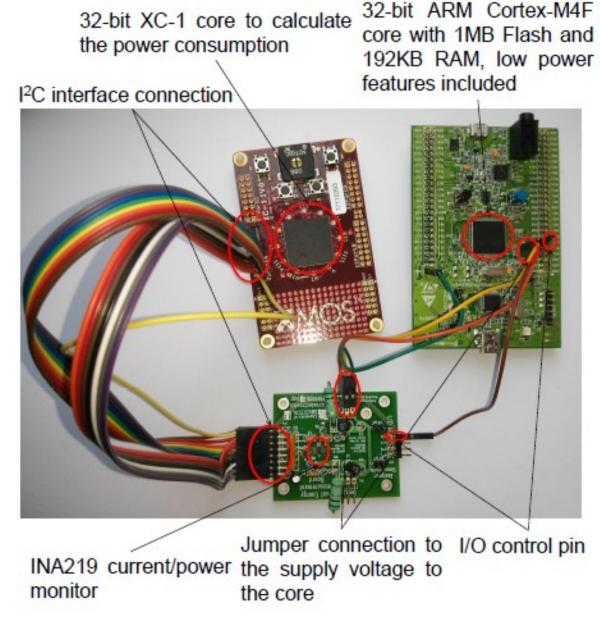
S. Kerrison and K. Eder, 2013. "Energy Modelling of Software for a Hardware Multi-threaded Embedded Microprocessor", under review at ACM TECS.







The Setup...



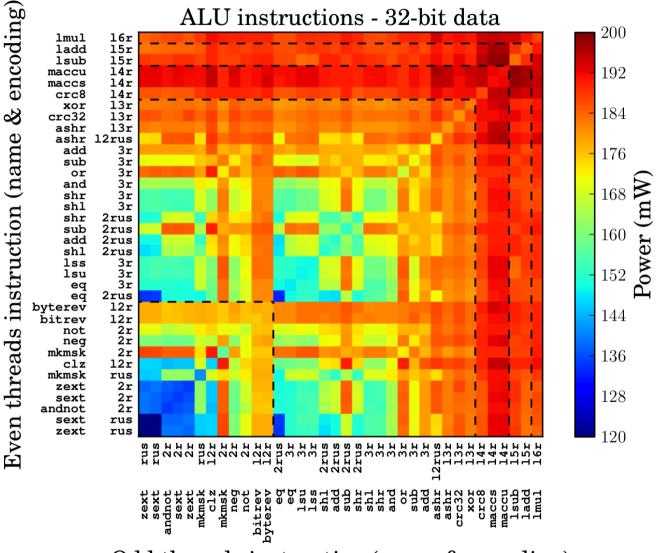








ISA Characterization



Odd threads instruction (name & encoding)

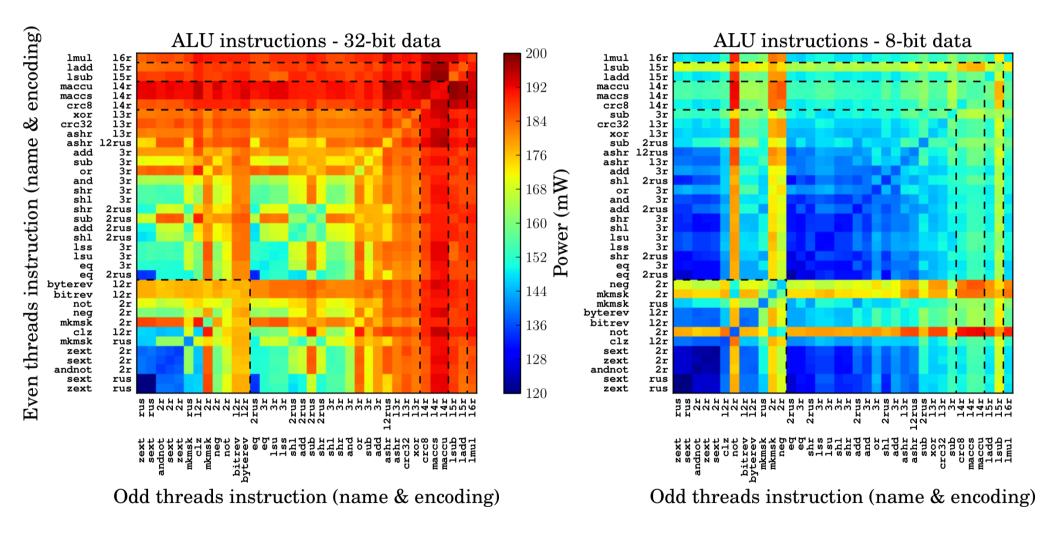








ISA Characterization

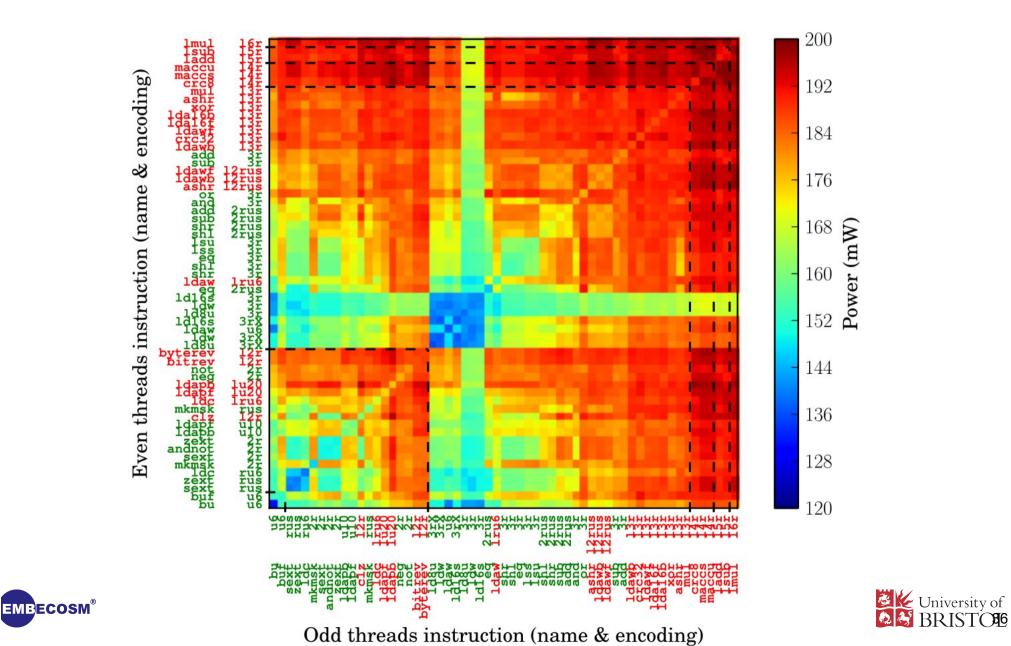








ISA Characterization



Resource Usage Analysis

Static Analysis for Energy Transparency and Optimization





Resource Usage Analysis

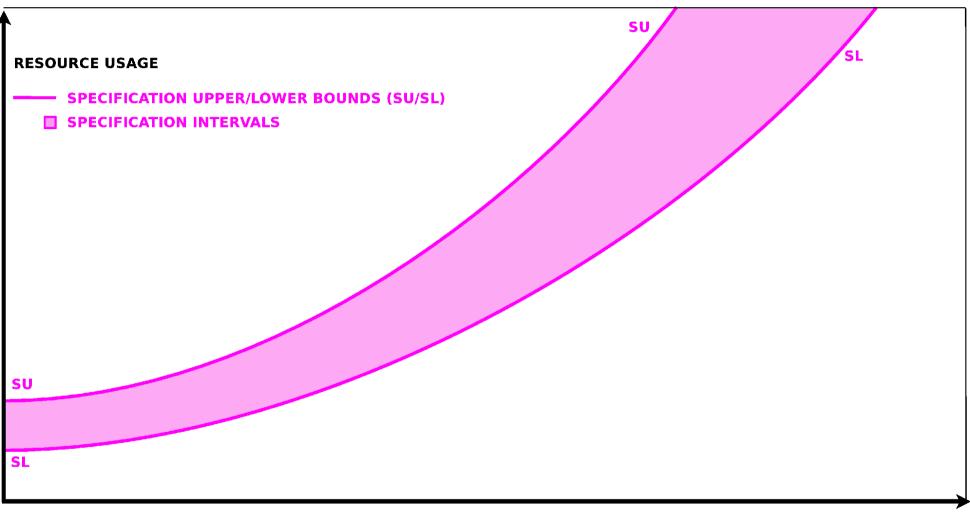
- Adaptation of advanced cost and WCET analysis techniques to energy consumption
- Techniques for automatically inferring both upper and lower bounds on energy usage of a procedure
- Bounds expressed using monotonic arithmetic functions per procedure depending on input data sizes or any other properties (e.g. location)
 - Bounds are safe and also as accurate as possible
- Verification can be done statically by checking if the upper and lower bounds on energy usage and any other resource defined in the specifications hold







Specified Resource Usage



INPUT DATA SIZE

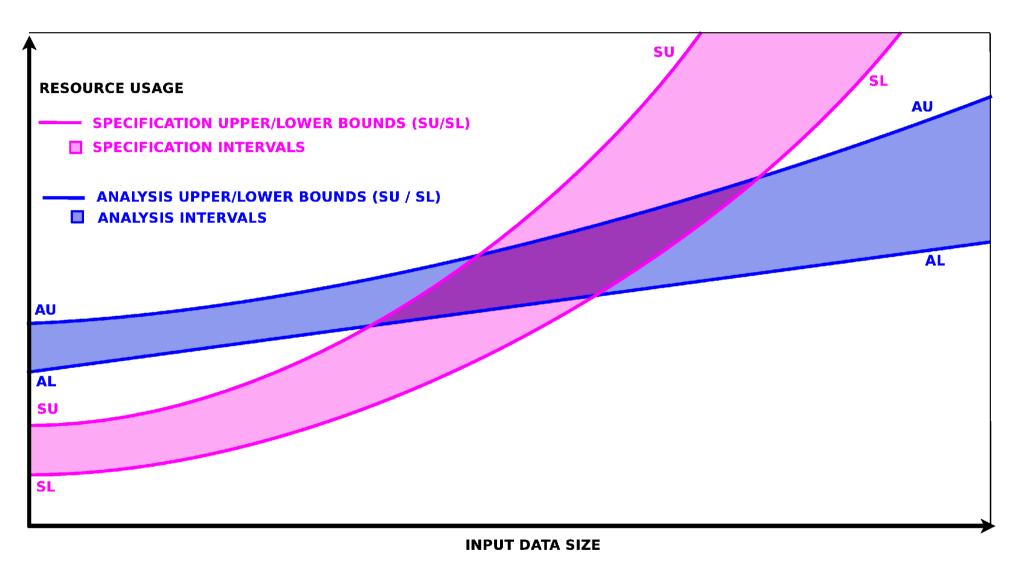
Source: Pedro Lopez Garcia, IMDEA Software Research Institute







Analysis Result



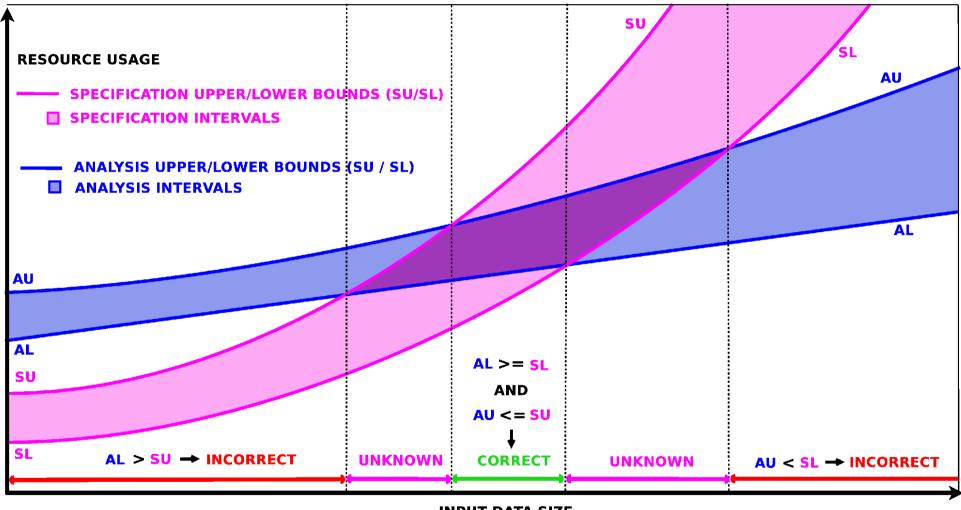
Source: Pedro Lopez Garcia, IMDEA Software Research Institute







Verification



INPUT DATA SIZE

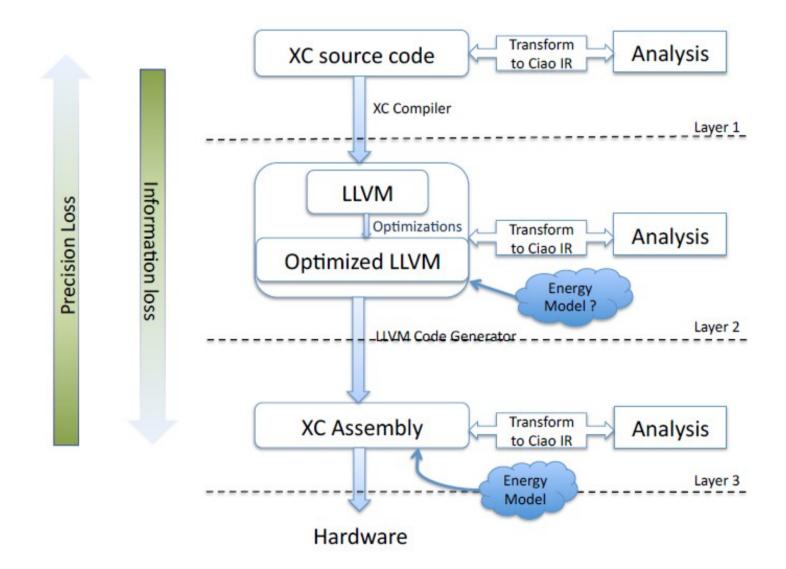
Source: Pedro Lopez Garcia, IMDEA Software Research Institute







Analysis Options

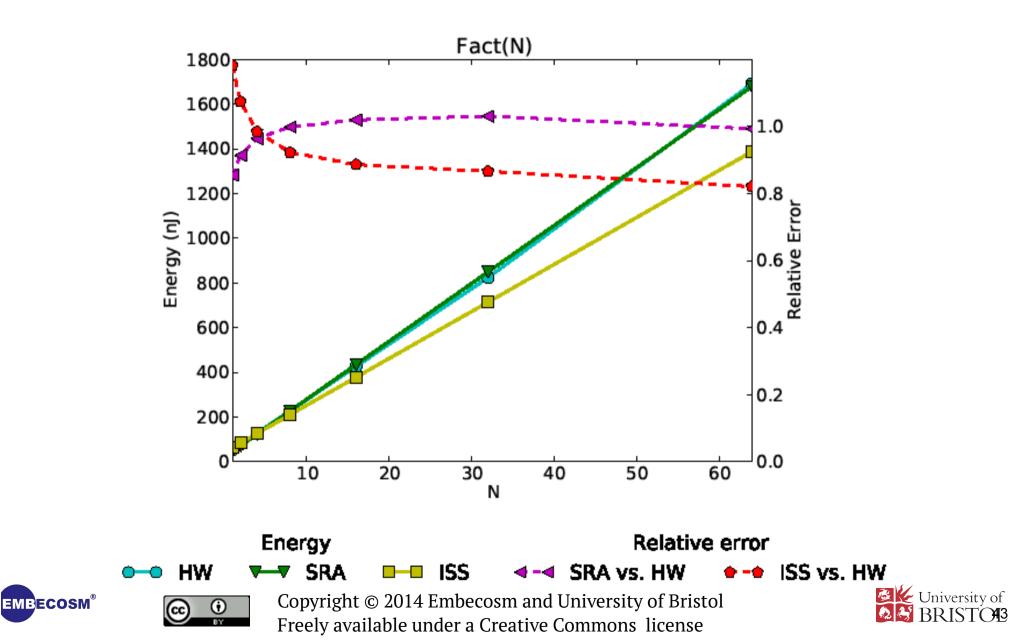




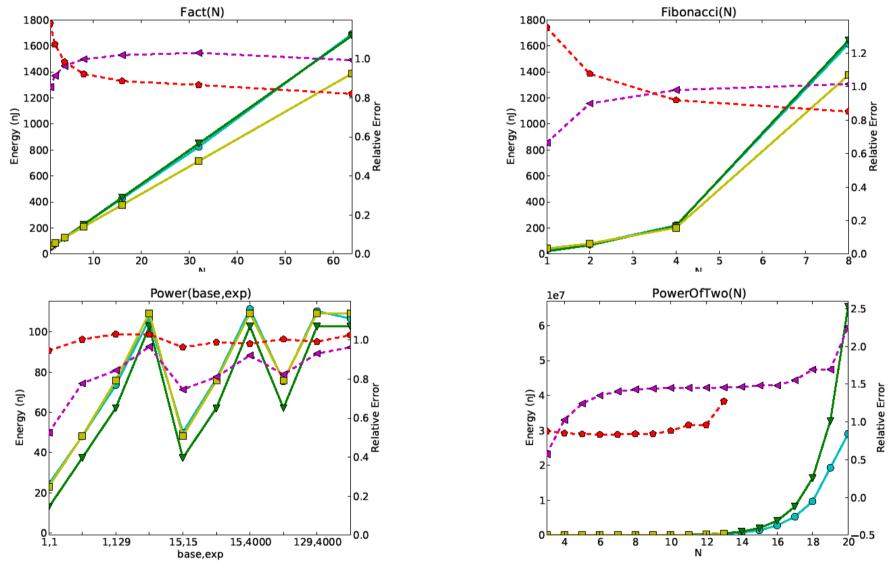




First Results



First Results



U. Liqat, S. Kerrison, A. Serrano, K. Georgiou, N. Grech, P. Lopez-Garcia, M.V. Hermenegildo and K. Eder. "Energy Consumption Analysis of Programs based on XMOS ISA-Level Models". LOPSTR 2013.







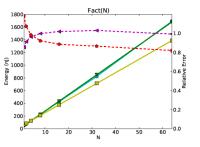
LLVM-IR to ISA Mapping

LLVM-IR	ISA			
LoopBody:				
%deref1 = load i32* %i				
store i32 %deref1, i32* %				
br label %LoopTest2, !dbg				
	.label10			
LoopBody3:	0x000100da: 05 5c:	ldw (ru6)	r0, sp[0x5]	
%3 = load i32* %numbers.bound	0x000100dc: 04 54:	stw (ru6)	r0, sp[0x4]	
%deref6 = load $[0 \times i32]^{**}$ %numbers	0x000100de: 20 73:	bu (u6)	0x20 <.label5>	
%deref7 = load i32* %j	.label8			
%boptmp8 = sub i32 %deref7, 1	0x000100e0: 08 5c:	ldw (ru6)	r0, sp[0x8]	
%subscript = getelementptr [0 x i32]* %deref6, i32 0, i32 %boptmp8	0x000100e2: 44 5c:	ldw (ru6)	r1, sp[0x4]	
%deref9 = load i32* %subscript	0x000100e4: 21 f8 ec		r2, r0[r1]	
%4 = load i32* %numbers.bound	0x000100e8: 68 9a:	sub (2rus)	r2, r2, 0x4	
%deref10 = load [0 x i32]** %numbers	0x000100ea: 28 08:	Idw (2rus)	and a second	
%deref11 = load i32* %j	0x000100ec: 01 48:		r2, r2[0x0]	
%subscript12 = getelementptr [0 x i32]* %deref10, i32 0, i32 %deref1		Idw (3r)	r0, r0[r1]	
%deref13 = load i32* %subscript12	0x000100ee: 02 c0:	lss (3r)	r0, r0, r2	
%relopcmp = icmp sgt i32 %deref9, %deref13	0x000100f0: 14 78:	bf (ru6)	r0, 0x14 <.label6>	
%cast = zext i1 %relopcmp to i32	0x000100f2: 00 73:	bu (u6)	0x0 <.label7>	
%zerocmp = icmp ne i32 %cast, 0				
br i1 %zerocmp, label %iftrue, label %ifdone				









• For HW designers:

"Power is a 1st and last order design constraint."

[Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]

"Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]



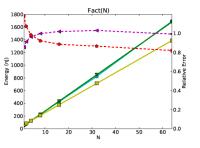
Scaling Power and the Future of CMOS

Mark Horowitz, EE/CS Stanford University









• For HW designers:

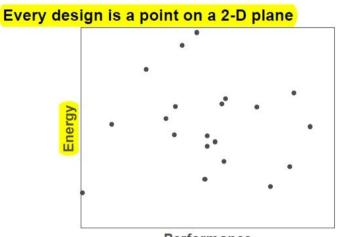
"Power is a 1st and last order design constraint."

[Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]

"Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]

Optimizing Energy

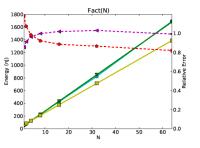


Performance









• For HW designers:

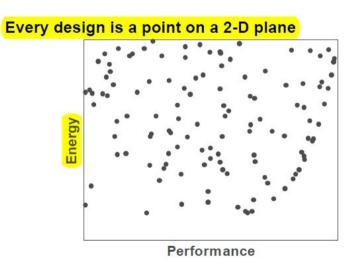
"Power is a 1st and last order design constraint."

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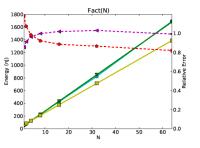
Optimizing Energy



EMBECOSM®







• For HW designers:

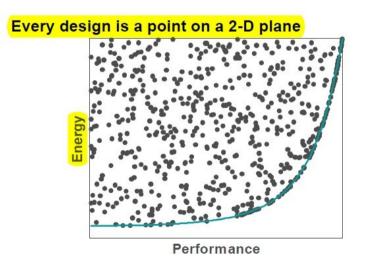
"Power is a 1st and last order design constraint."

[Dan Hutcheson, VLSI Research, Inc., E³S Keynote 2011]

"Every design is a point in a 2D plane."

[Mark Horowitz, E³S 2009]

Optimizing Energy



EMBECOSM®





More POWER to SW Developers

in 15ms do {...}
in 29000uJ do
{...}

- Energy Transparency from HW to SW
- Location-centric programming model
 - "Cool" code A cool programming competition!

Promoting energy efficiency to a 1st class SW design goal is an urgent research challenge.





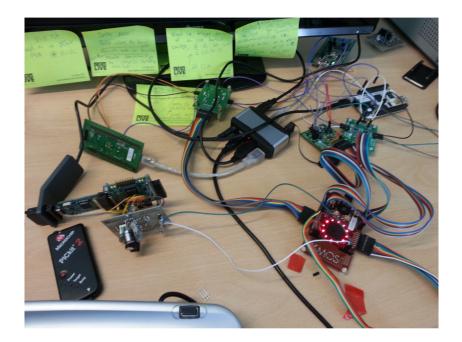


The Impact of Compilers on Energy Usage





Do Compilers Affect Energy?



- Initial research in 2012 by Embecosm and Bristol University
- Now published <u>open access</u> in a peer-reviewed journal

Identifying Compiler Options to Minimize Energy Consumption for Embedded Platforms James Pallister; Simon J. Hollis; Jeremy Bennett The Computer Journal 2013; doi: 10.1093/comjnl/bxt129 http://comjnl.oxfordjournals.org/cgi/reprint/bxt129?ijkey=aA4RYIYQLNVgkE3







What is MAGEEC?







Today we optimize for speed or space

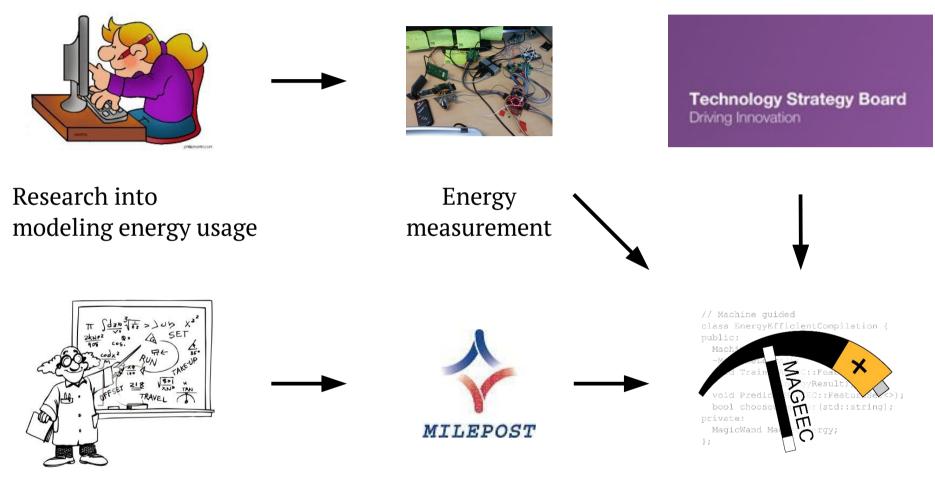
What if we could optimize for energy usage?







MAchine Guided Energy Efficient Compilation



Research into feedback directed optimization



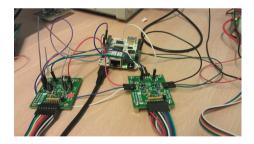




What's New?



Objective is energy optimization



Energy measured *not* modeled



Generic framework: GCC *and* LLVM initially



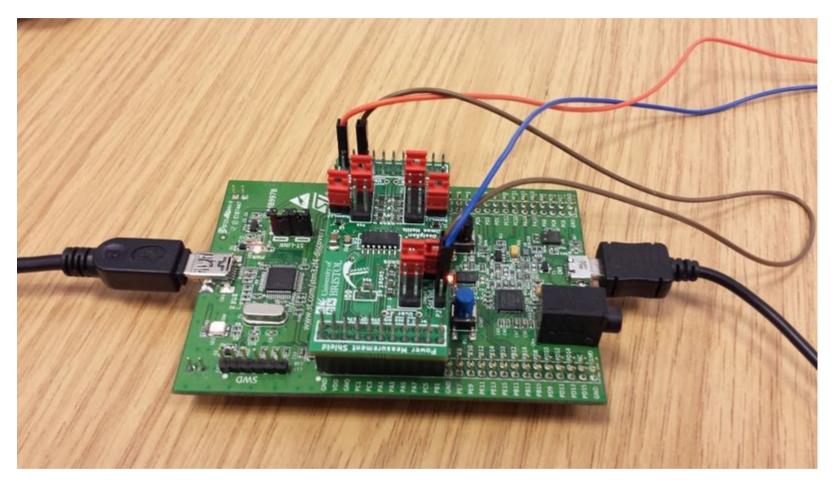
Working system, not research prototype







A Free and Open Source Energy Measurement System



mageec.org/wiki/Power_Sensing_Board







BEEBS

The <u>Bristol/Embecosm</u> <u>Embedded</u> <u>Benchmark</u> <u>Suite</u>

- A free and open source benchmark suite for embedded systems
 - expose different energy consumption characteristics
 - one benchmark can't trigger all optimisations
 - broad categories to be considered
 - integer, floating point, branch frequency, memory bandwidth

Name	Source	В	\mathbf{M}	Ι	\mathbf{FP}	Т	License	Category
Blowfish	MiBench	\mathbf{L}	Μ	Η	L	Multi	GPL	security
CRC32	MiBench	Μ	\mathbf{L}	Η	\mathbf{L}	Single	GPL	network, telecomm
Cubic root solver	MiBench	\mathbf{L}	\mathbf{M}	Η	\mathbf{L}	Single	GPL	automotive
Dijkstra	MiBench	Μ	\mathbf{L}	Η	\mathbf{L}	Multi	GPL	network
FDCT	WCET	Η	Η	\mathbf{L}	Η	Single	None^\dagger	consumer
Float Matmult	WCET	\mathbf{M}	Η	Μ	\mathbf{M}	Single	GPL	automotive, consumer
Integer Matmult	WCET	Μ	Μ	Η	\mathbf{L}	Single	None^{\dagger}	automotive
Rjindael	MiBench	Η	\mathbf{L}	Μ	\mathbf{L}	Multi	GPL	security
SHA	MiBench	Η	\mathbf{M}	Μ	\mathbf{L}	Multi	GPL	network, security
2D FIR	WCET	Η	Μ	\mathbf{L}	Η	Single	$\operatorname{None}^{\dagger}$	automotive, consumer







Get Involved





Get Involved at FOSDEM

Developer room on Sunday

Energy Efficent Computing

Start 9:00am, Room AW1.26







Energy-efficient computing devroom

Room: AW1.126

09	1	0	11	12	2	13	14	15	16	17	18	
Sunday En W	Meas	An	spEEDO:	Op	Or Meas	uring applica	ation energ	ју со	MAGE MAchi EA			

Event	Speakers	Start	End						
Sunday									
Energy scavenging, battery life and should we build more power stations Why energy-efficiency of hardware and software matters	Jeremy Bennett	09:00	09:30						
Measuring energy consumption in embedded systems	Simon Hollis	09:30	10:15						
An approach for energy consumption analysis of programs using LLVM	Kerstin Eder, Kyriakos Georgiou, Neville Grech	10:15	10:45						
spEEDO: Energy Efficiency through Debug suppOrt	David Greaves	10:45	11:45						
Open Energy Measurement Hardware	James Pallister	11:45	12:15						
Open Low Power Devices meet the mbed open platform	Emilio Monti	12:15	12:30						
Measuring application energy consumption with instrumented hardware (workshop)	Andrew Back, Jeremy Bennett, Kerstin Eder, Simon Hollis, James Pallister, Simon Cook	12:30	15:30						
MAGEEC MAchine Guided Energy Efficient Compilation	Simon Cook	15:30	16:15						
EACOF: The Energy-Aware COmputing Framework	Hayden Field, Kerstin Eder, James Pedlingham	16:15	16:45						







Get Involved After FOSDEM

- MAGEEC
 - website: http://mageec.org/
 - wiki: http://mageec.org/wiki/MAGEEC
 - mailing list: http://mageec.org/cgi-bin/mailman/listinfo/mageec
- EACOF: https://github.com/eacof/eacof
- ENTRA: http://entraproject.eu/
- University of Bristol
 - PhD, summer projects, secondments, industrial collaborators.
 - EACO initiative: http://www.cs.bris.ac.uk/Research/Micro/eaco.jsp
- Embecosm: now hiring







Technology Strategy Board Driving Innovation

// Machine guided
class EnergyEfficientCompilation {
public:
 Machine guided
 rain the critical of the critical of





XMOS®



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Thank You For Your Attention

Kerstin.Eder@bristol.ac.uk Jeremy.Bennett@embecosm.com