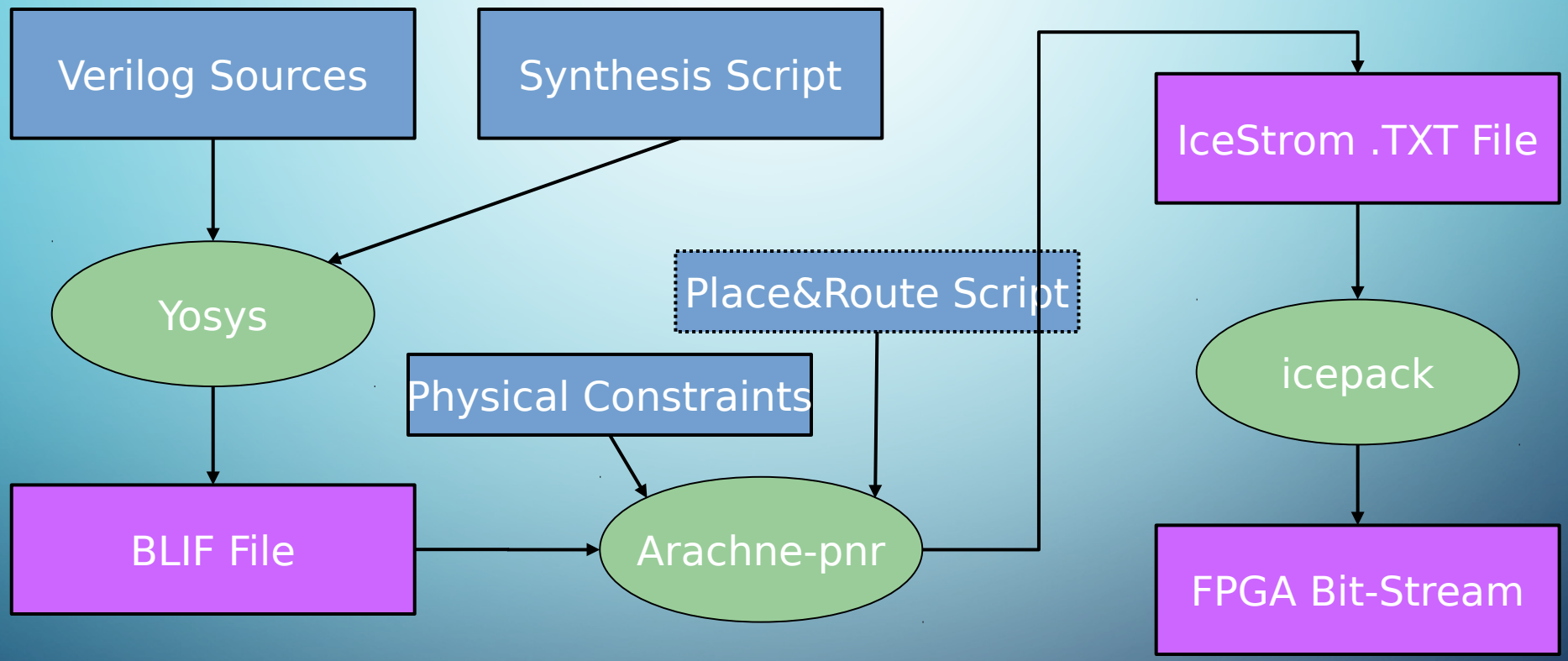
OPEN SOURCE FPGA TOOLCHAIN

WHY IF VIVADO AND QUARTUS ARE „FREE“ ANYWAY

WHOAMI

- Open Source Evangelist
- Team: Clifford Daniel Edmund

WHAT DO WE HAVE: FPGA TOOLCHAIN



	Yosys Arachne-pnr	Synplify Pro SBT Backend	Lattice LSE SBT Backend
Packed LCs	2996	2647	2533
LUT4	2417	2147	2342
DFF	1005	1072	945
CARRY	497	372	372
RAM4K	8	7	8
Synthesis Time	30 seconds	30 seconds	21 seconds
Implementation Time	81 seconds	405 seconds	415 seconds

Design	Timing Tool	Yosys Arachne-pnr (unconstrained)	Lattice LSE SBT Backend (constr. 100 MHz)
PicoRV32_AXI (w/ reduced pin count)	`sbtime`	N/A	41.74 MHz
	`icetime -i`	54.33 MHz	41.75 MHz
	`icetime -im`	53.02 MHz	41.40 MHz
Navre AVR Clone (from Milkymist SoC)	`sbtime`	N/A	45.82 MHz
	`icetime -i`	29.89 MHz	45.59 MHz
	`icetime -im`	27.61 MHz	44.90 MHz
Whishbone SPI Core (from OpenCores)	`sbtime`	N/A	62.13 MHz
	`icetime -i`	42.62 MHz	62.23 MHz
	`icetime -im`	38.89 MHz	61.14 MHz

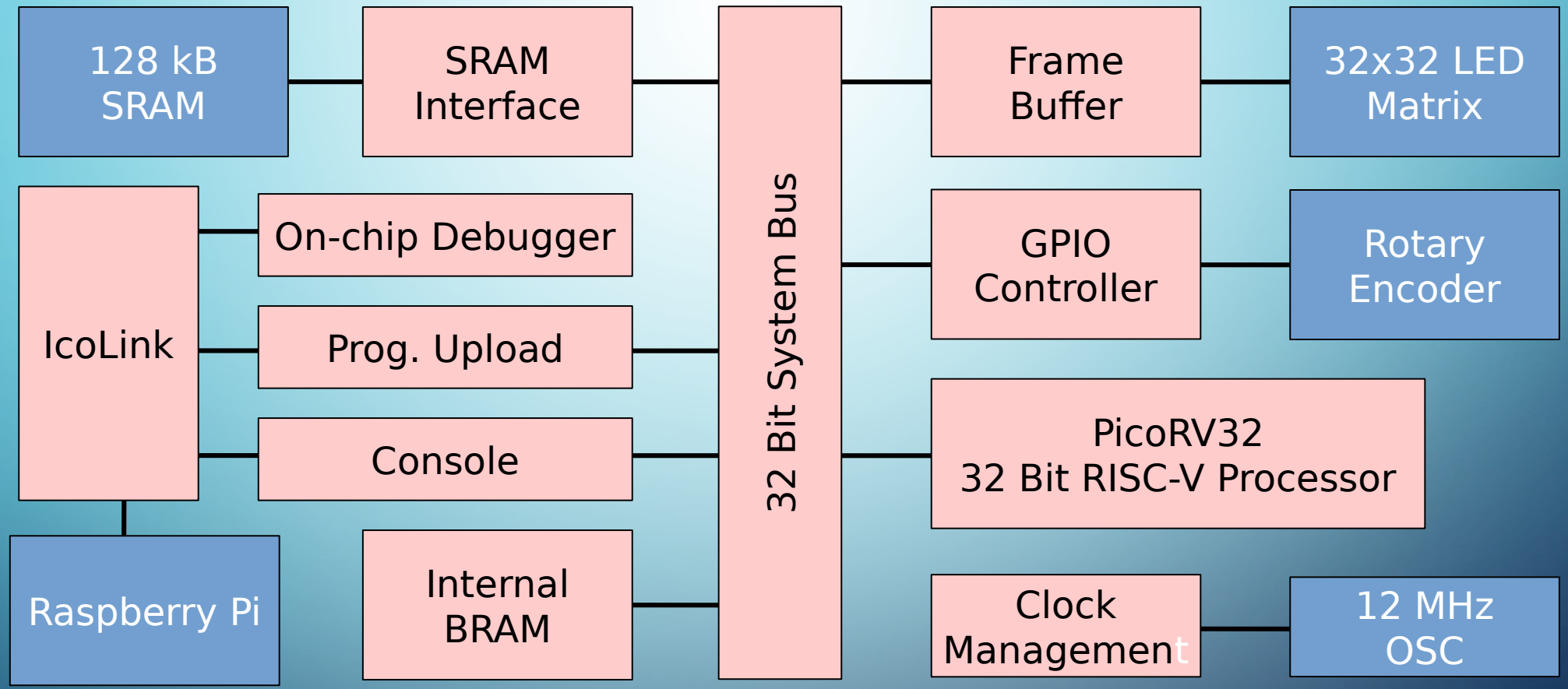
WHAT DO WE HAVE: BOARDS

- Lattice ICEstick 1k (21 USD)
- Lattice evaluation board 8k LUT (42 USD)
- IcoBoard 8k LUT , 1 Mb SRAM, Flash (90 Euro)
- Olimex, BQ

WHAT DO WE HAVE: Verilog IP BLOCKS

- CPUs
- SRAM, SPI, UART, I2C, …
- Minimal Risc-V SoC

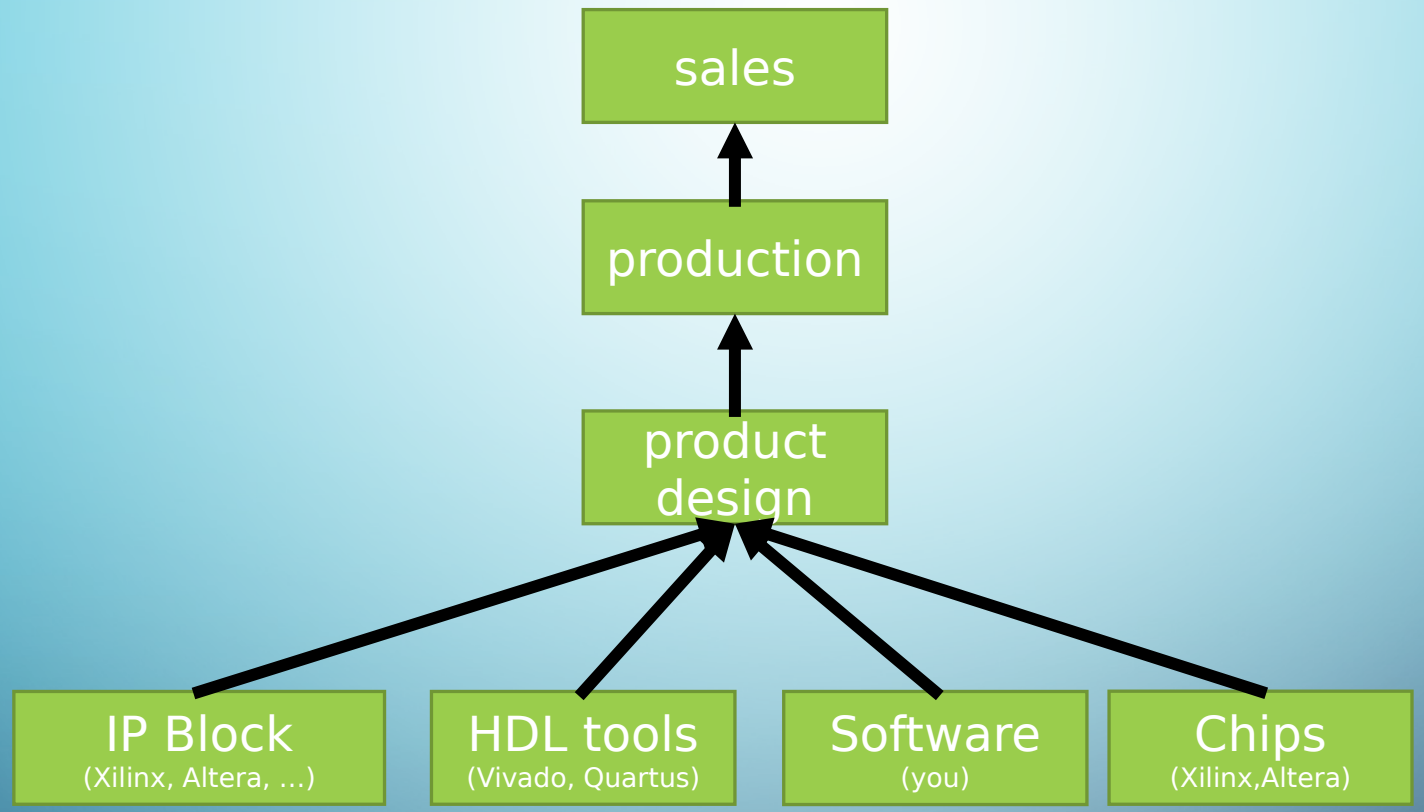
Demo SoC – Simplified Block Diagram

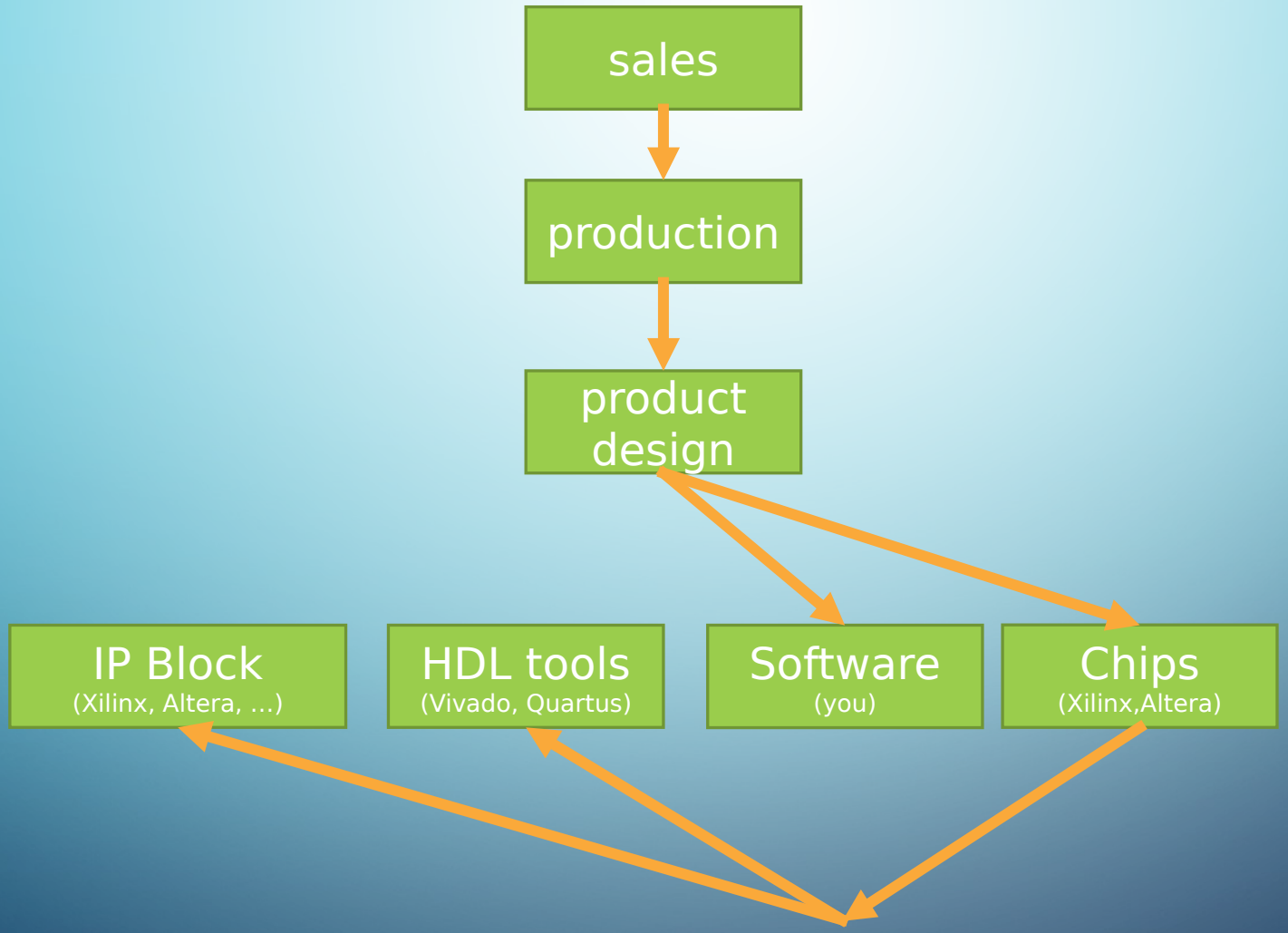


OPEN SOURCE TOOLCHAIN: WHY CARE?

- learning
- innovation
- Integration
- wastefull IP

The Industry


sales
production
product design
IP Block
(Xilinx, Altera, ...)
HDL tools
(Vivado, Quartus)
Software
(you)
Chips
(Xilinx,Altera)


sales
production
product design
IP Block
(Xilinx, Altera, ...)
HDL tools
(Vivado, Quartus)
Software
(you)
Chips
(Xilinx,Altera)

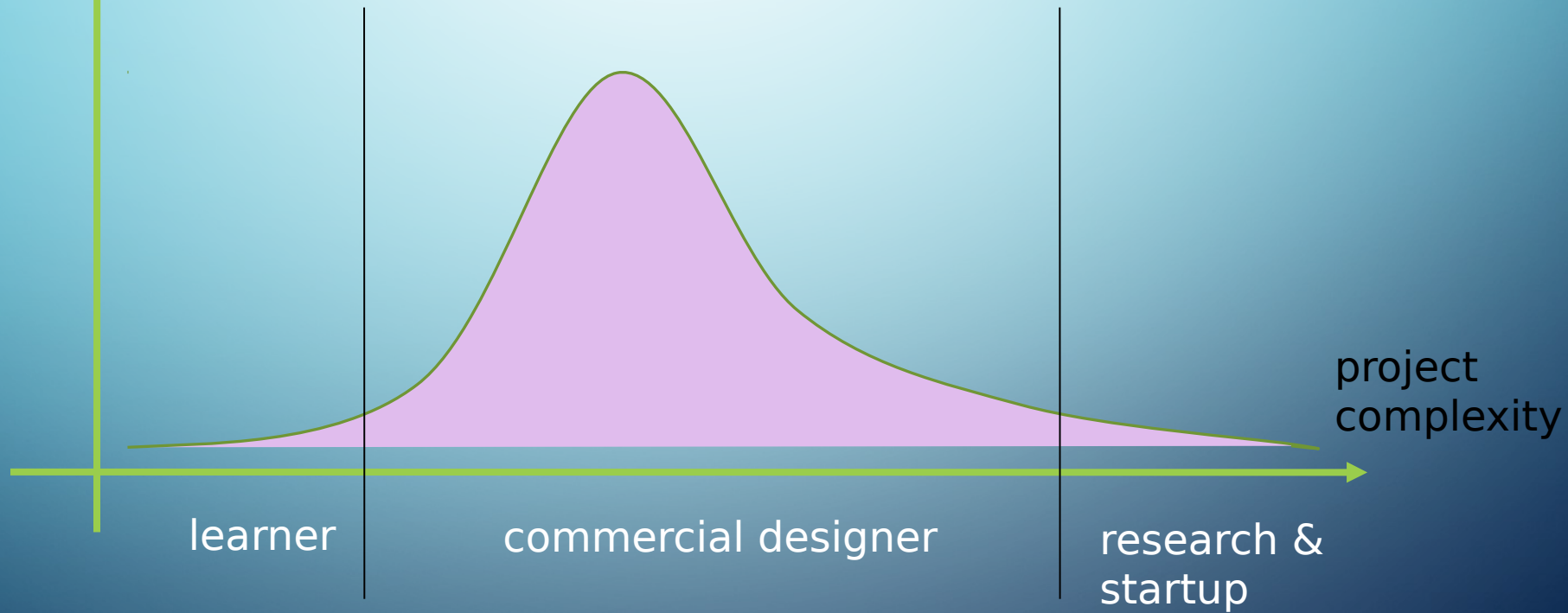
GOAL:

make money by moving many chips

number of chips sold

„we make tools for the guys who move chips“

„design win!“



Learners dont buy many chips

==> manufacturer do not listen/invest in their requirements

tools are too powerfull
tools are too complicated

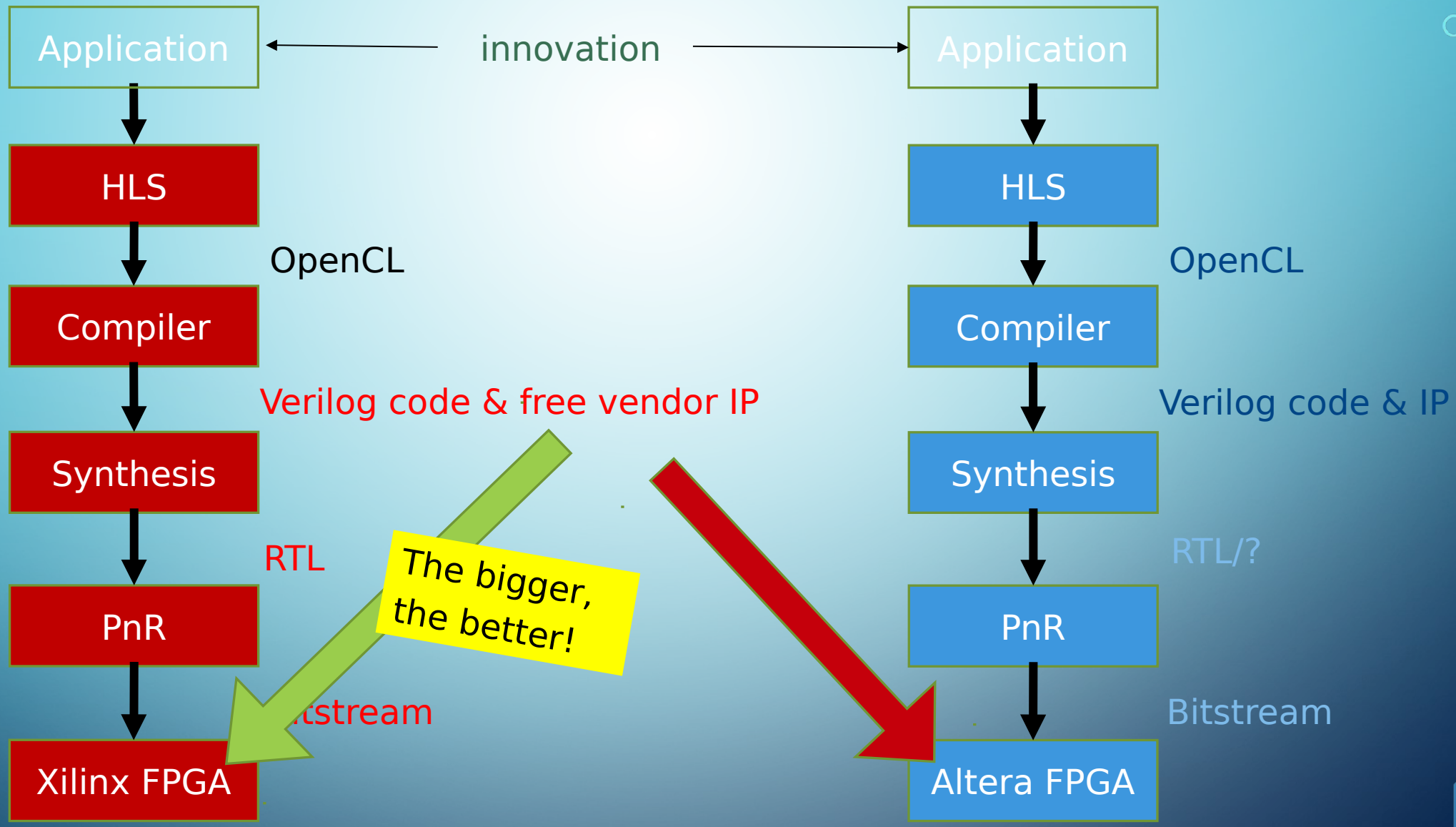
Chipmakers do not make money on innovative high added value designs.

Innovators only move small number of chips

==> no good toolsupport for innovation

➔ LITTLE TOOL INNOVATION

- No new programming tools
  (Verilog was started 1984, Perl was started 1987)
- No new usecases (which usually start out small)
- .....


Application
innovation
Application
HLS
OpenCL
HLS
OpenCL
Compiler
Compiler
Verilog code & free vendor IP
Verilog code & IP
Synthesis
Synthesis
RTL
RTL/?
The bigger, the better!
PnR
PnR
tstream
Bitstream
Xilinx FPGA
Altera FPGA

- makes cross vendor integration hard and expensive
- Is In the interest of Altera and Xilinx
- They love „lock in“, not sharing, reuse and innovation

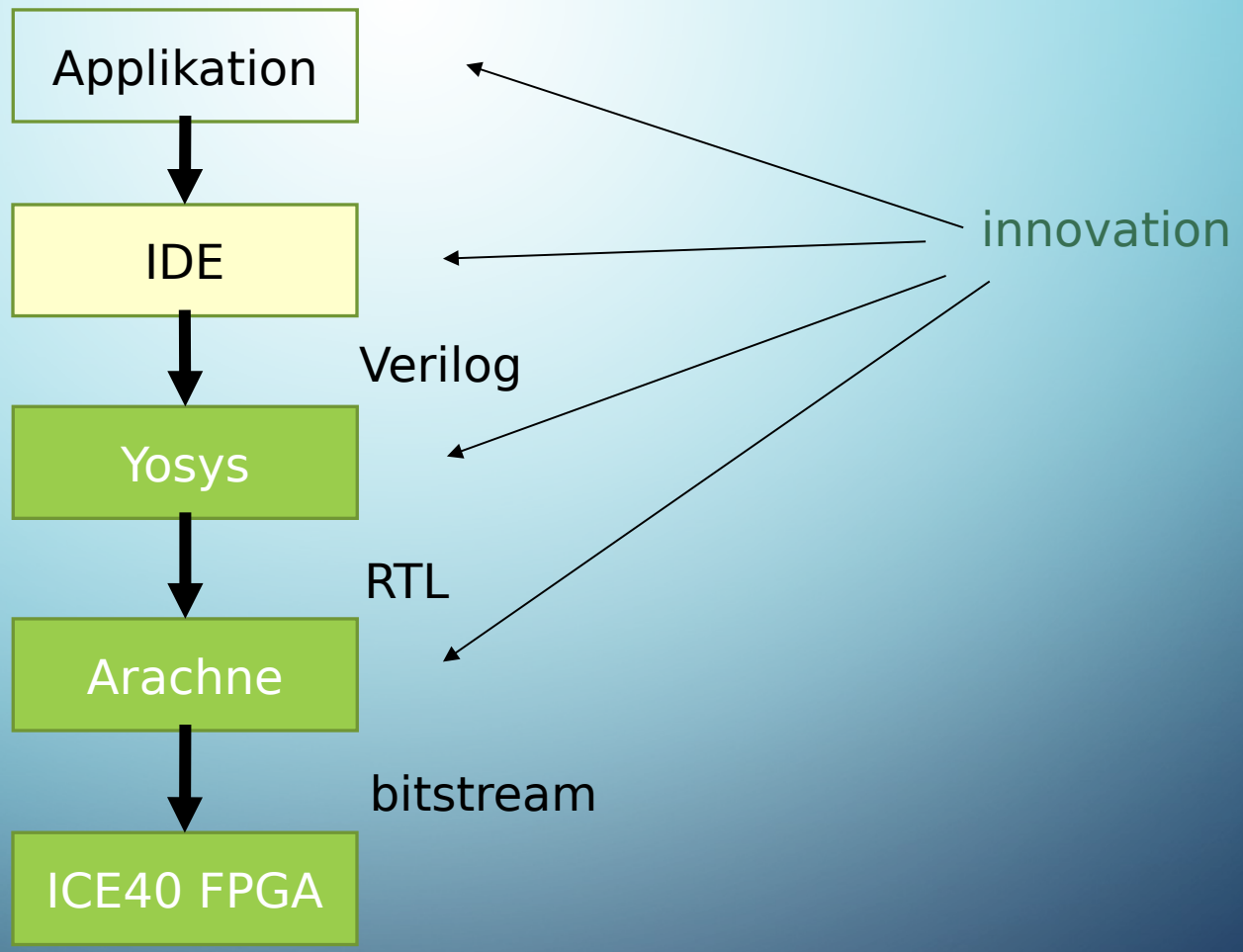
Green walled gardens of

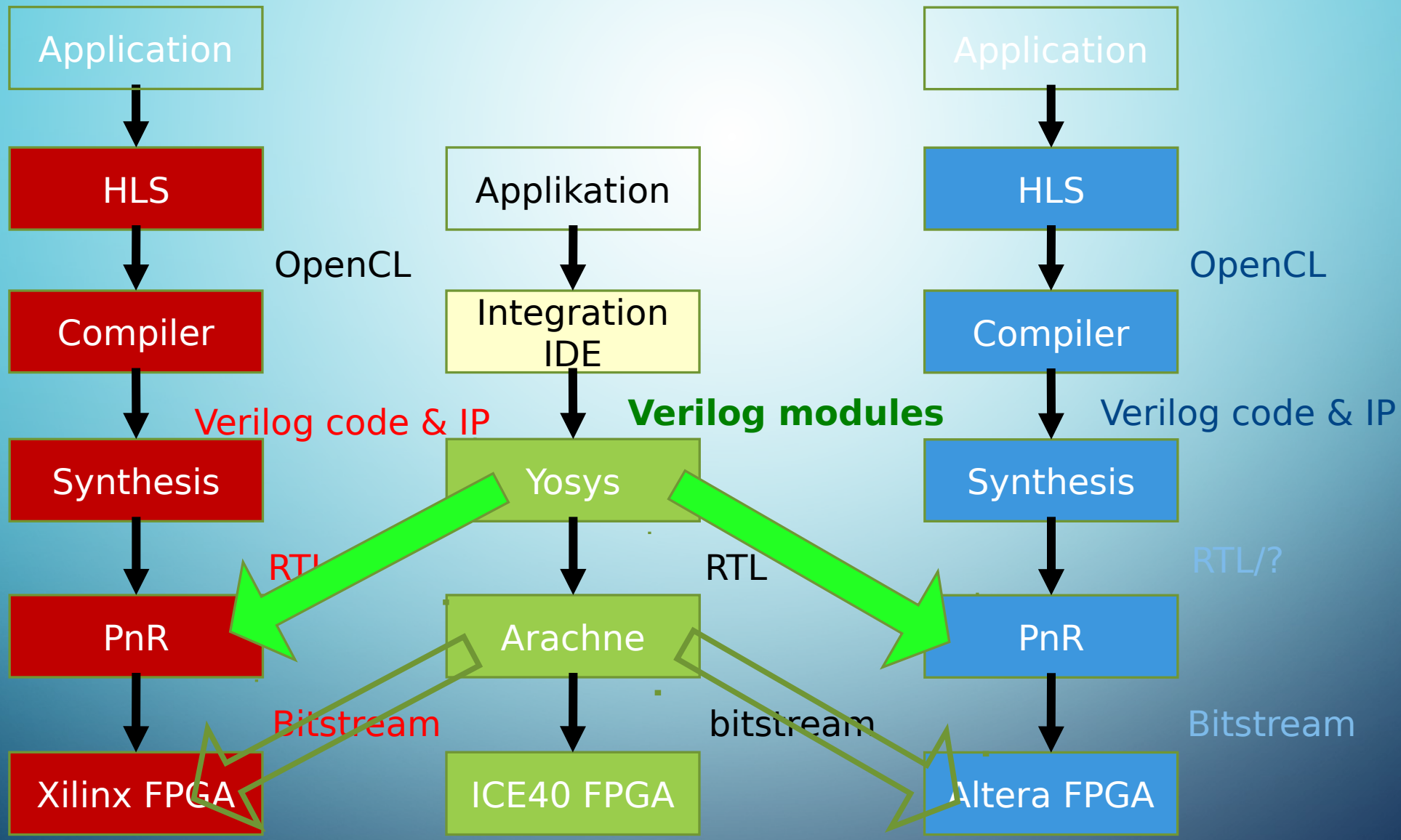
Xilinx and Altera.

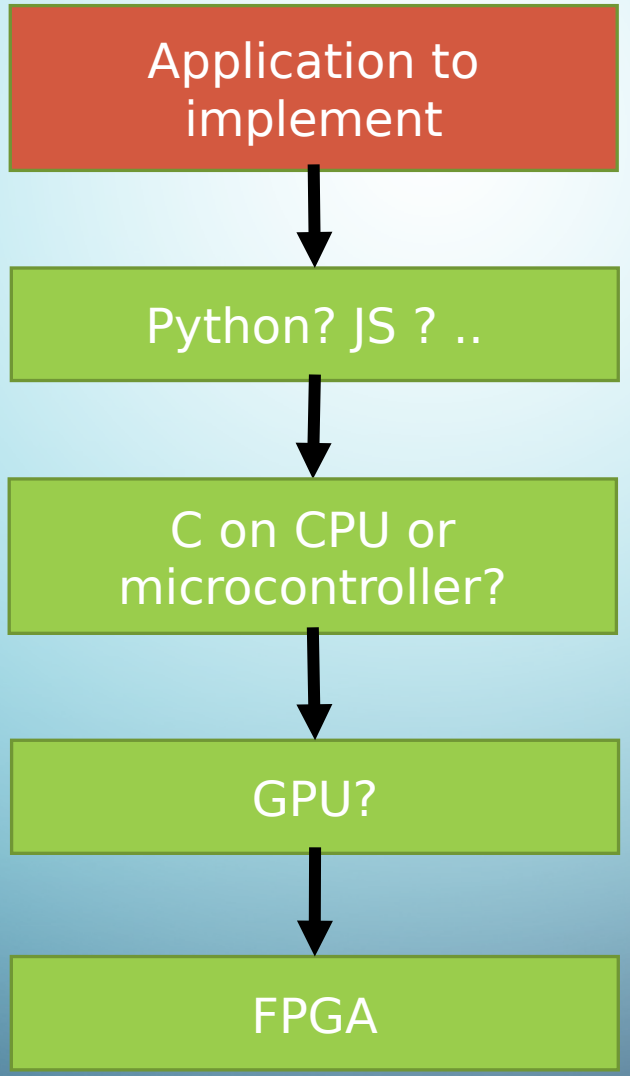
Think „Unix wars“

For an innovation very often you have to touch the whole stack

- If a part of stack is propriety, this component determines the speed of innovation.
- With open compenents, innovation can go forward faster.
- There would be no Facebook without Linux.


Applikation
IDE
Verilog
Yosys
RTL
Arachne
bitstream
ICE40 FPGA
innovation


Application
HLS
OpenCL
Compiler
Verilog code & IP
Synthesis
RTL
PnR
Bitstream
Xilinx FPGA
Applikation
Integration IDE
Verilog modules
Yosys
RTL
Arachne
bitstream
ICE40 FPGA
Application
HLS
OpenCL
Compiler
Verilog code & IP
Synthesis
RTL/?
PnR
Bitstream
Altera FPGA



FPGA is hard!

Use it only if you need to!

- Application has requirememement for low latency

Application has a huge bandwith-requirement and a streamable solution

- Application has requirement for precise timing

USECASES for Lattice ICE40

- digital design education
- research
- control-systems
- dynamic trigger in logic analyser
- signal predistortion, fast sensordata processing

...

- embedded bitstream generation

We are looking ...

- to grow the eco system
- to write open/free Verilog blocks
- to have great demo usecases
- to support larger/faster FPGAs
- for learners and innovators
- to develop an integrated IDE to ease integration

More technical presentation:

Clifford Wolf: Author of Yosys

AW1.121 EDA developer room today 14:00

Q & A ...

http://icoboard.org