Qucs
Quite Universal Circuit Simulator

Overview, Status and Roadmap

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FOSDEM 2016
EDA Developer room
Brussels, 30 January 2016

Qucs /kju:ks/

- Overview
  - Project background
  - Package contents
  - What can you do with?
  - Demo
- Status
  - Development
  - Next release
- Roadmap
  - Our whishes for the future

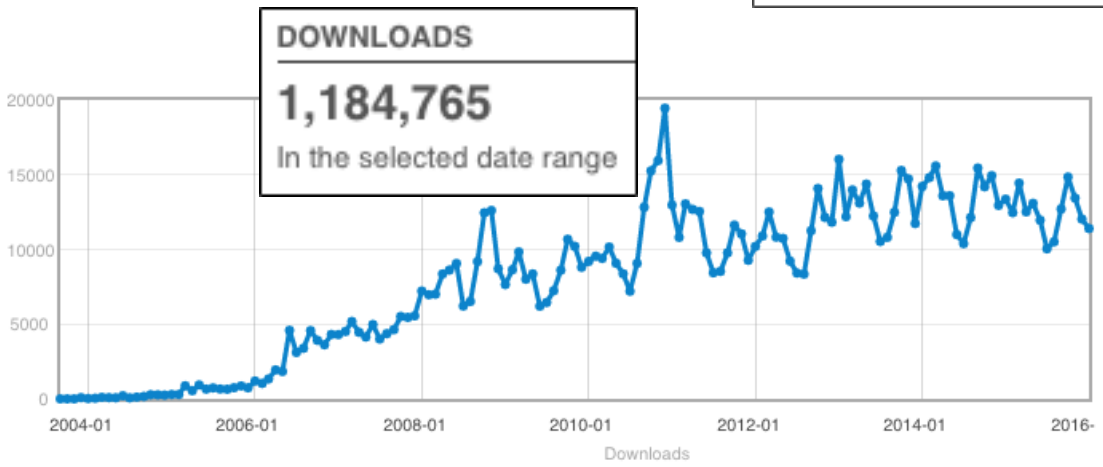
Project background

- Started in 2003
  - Michael Margraf
  - Stefan Jahn
- GPLv2+
- 20+ contributors
- 20 languages
- Cross-platform
- Users
  - Education
  - Research
  - Hobbyists
  - Industry

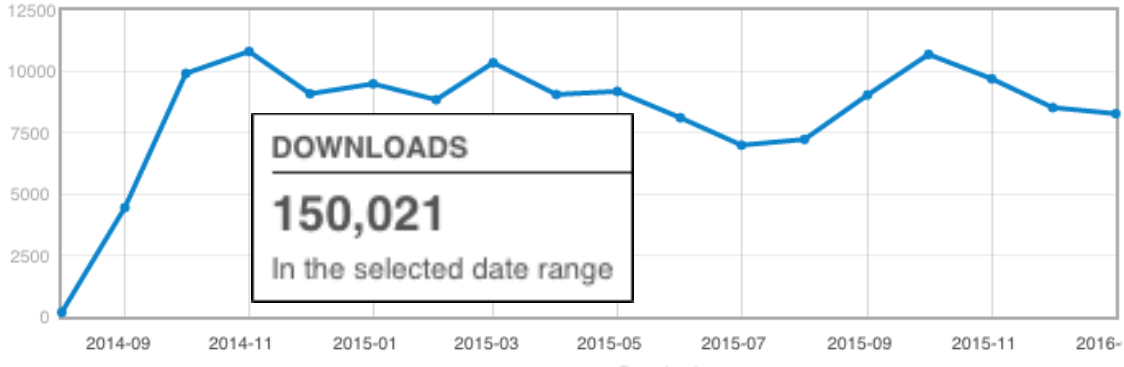
Web counter

1300575
visitors since 2005/04/27

- 2003 … 2016



- Qucs 0.0.18 - Windows



Package contents

- (sort of an) IDE
- Schematic capture
- Simulation tools
  - Qucsator
  - Optimizer (ASCO)
  - Icarus-Verilog
  - FreeHDL
- Data visualization
- Equation system
- Component library
- Design / synthesis tools

- Extensible
  - Spice import
  - Verilog-A model builder
  - Octave/MATLAB

- Dependencies
  - C++ compiler
  - Qt4 (with Qt3Support)
  - Autotools / CMake
  - gperf / flex / bison
  - ADMS
  - LaTex

Support

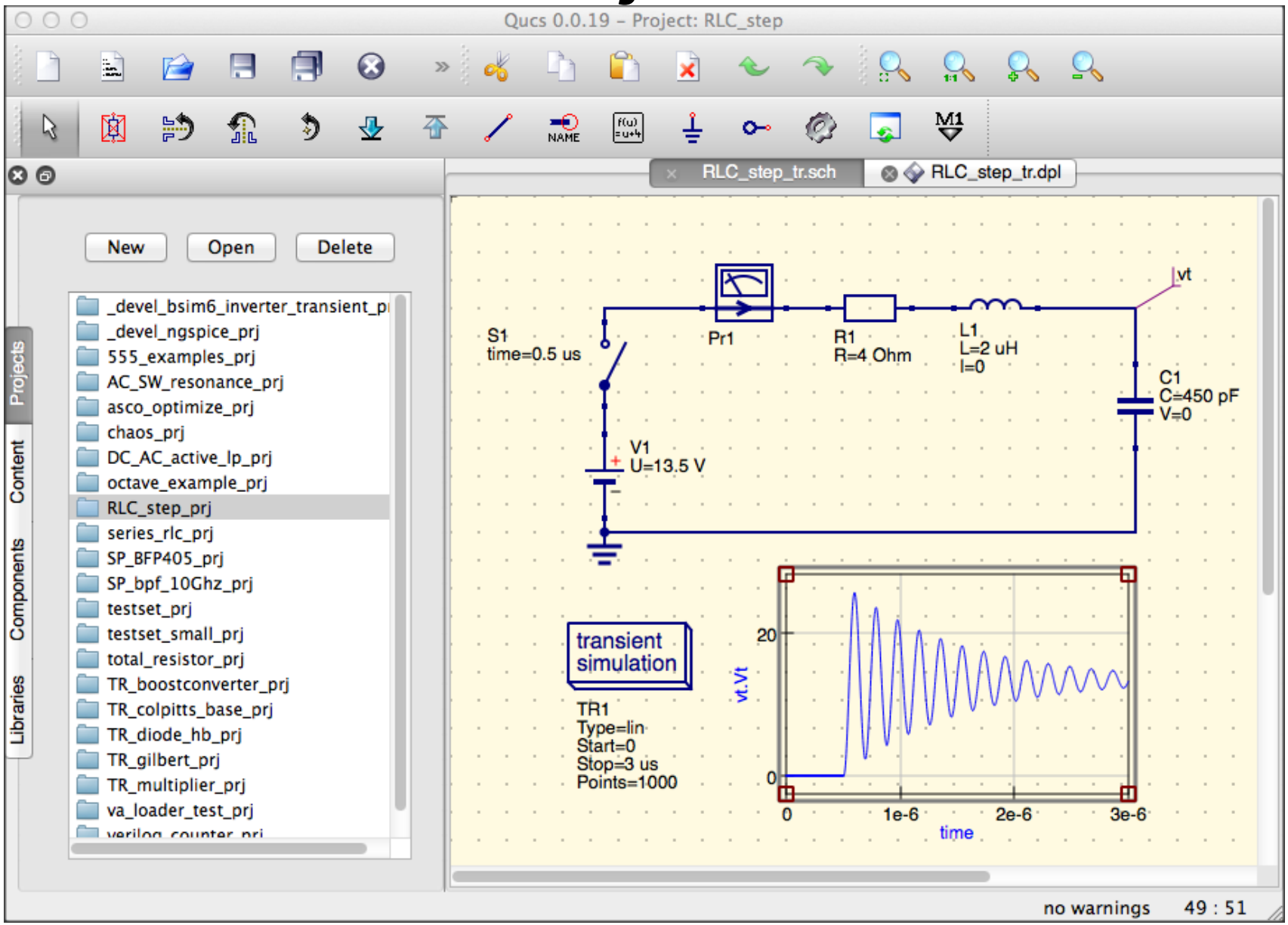
- Website
  http://qucs.sourceforge.net
- Current developers: ~ 6
- Documentation
  - Help
  - Tutorial Workbook
  - Report Workbook
  - Technical Manual
- SourceForge
  - Binaries
  - Git repository (mirror)
  - Issue tracker
  - Forum / mailing lists
- GitHub
  - Git repository (preferred)
  - Issue tracker
  - Wiki
  - Travis CI
  - AppVeyor
  - Coveralls

Tools

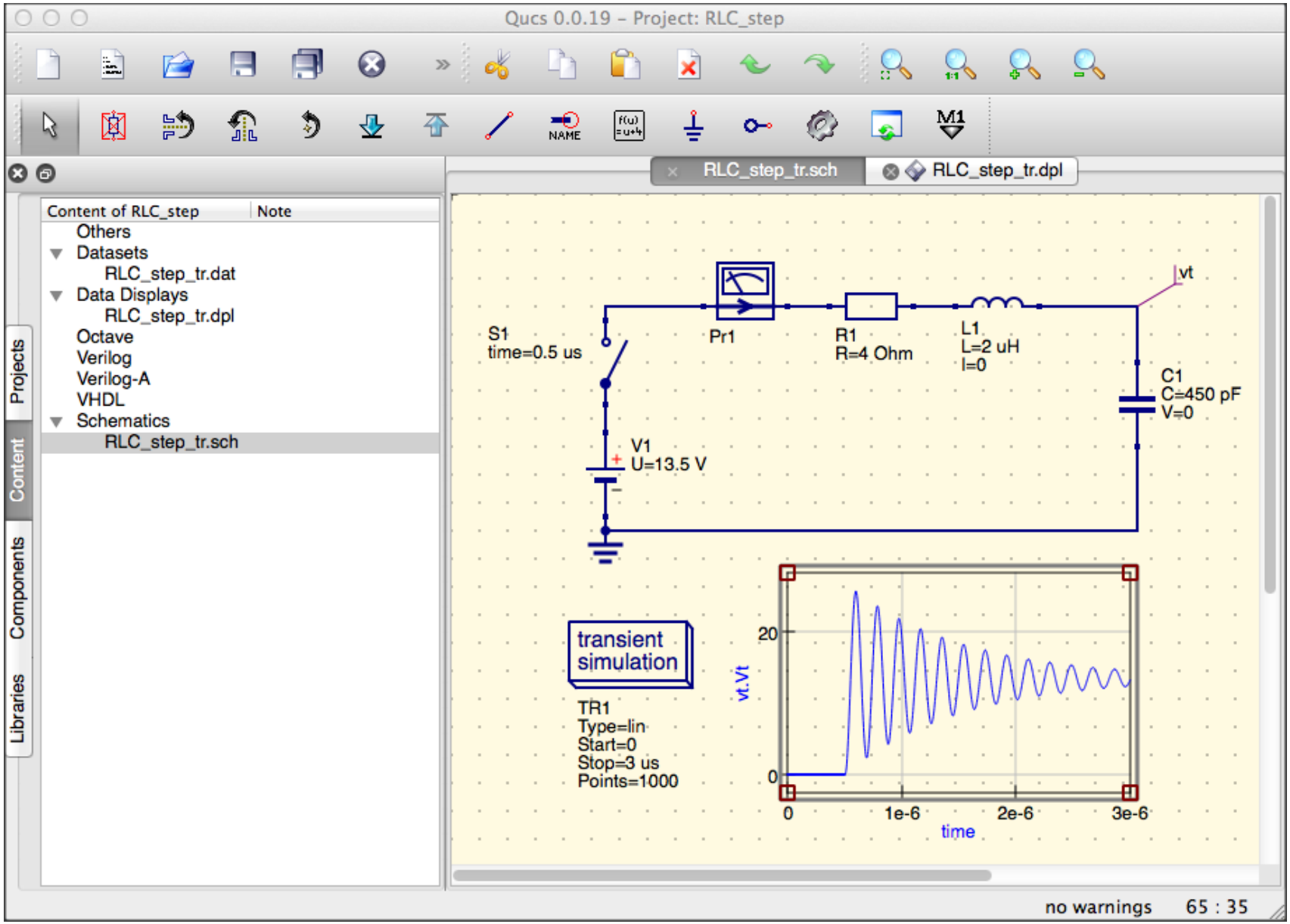
- Graphical Interface
  - Qucs
  - ActiveFilter
  - Attenuator
  - Editor
  - Filter
  - Help
  - Matching
  - Library
  - Rescodes
  - Transcalc
- ~ 170 components

- Command Line
  - qucs
  - qucsator
  - qucsconv
- Third-party and scripts
  - asco
  - admsXml
  - iverilog
  - freehdl
  - ps2sp
  - octave
  - python

Projects


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
New
Open
Delete
_devel_bsim6_inverter_transient_p
_devel_ngspice_prj
555_examples_prj
AC_SW_resonance_prj
asco_optimize_prj
chaos_prj
DC_AC_active_lp_prj
octave_example_prj
RLC_step_prj
series_rlc_prj
SP_BFP405_prj
SP_bpf_10Ghz_prj
testset_prj
testset_small_prj
total_resistor_prj
TR_boostconverter_prj
TR_colpitts_base_prj
TR_diode_hb_prj
TR_gilbert_prj
TR_multiplier_prj
va_loader_test_prj
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
49 : 51

Contents


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
Content of RLC_step
Note
Others
Datasets
RLC_step_tr.dat
Data Displays
RLC_step_tr.dpl
Octave
Verilog
Verilog-A
VHDL
Schematics
RLC_step_tr.sch
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
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L=2 uH
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vt
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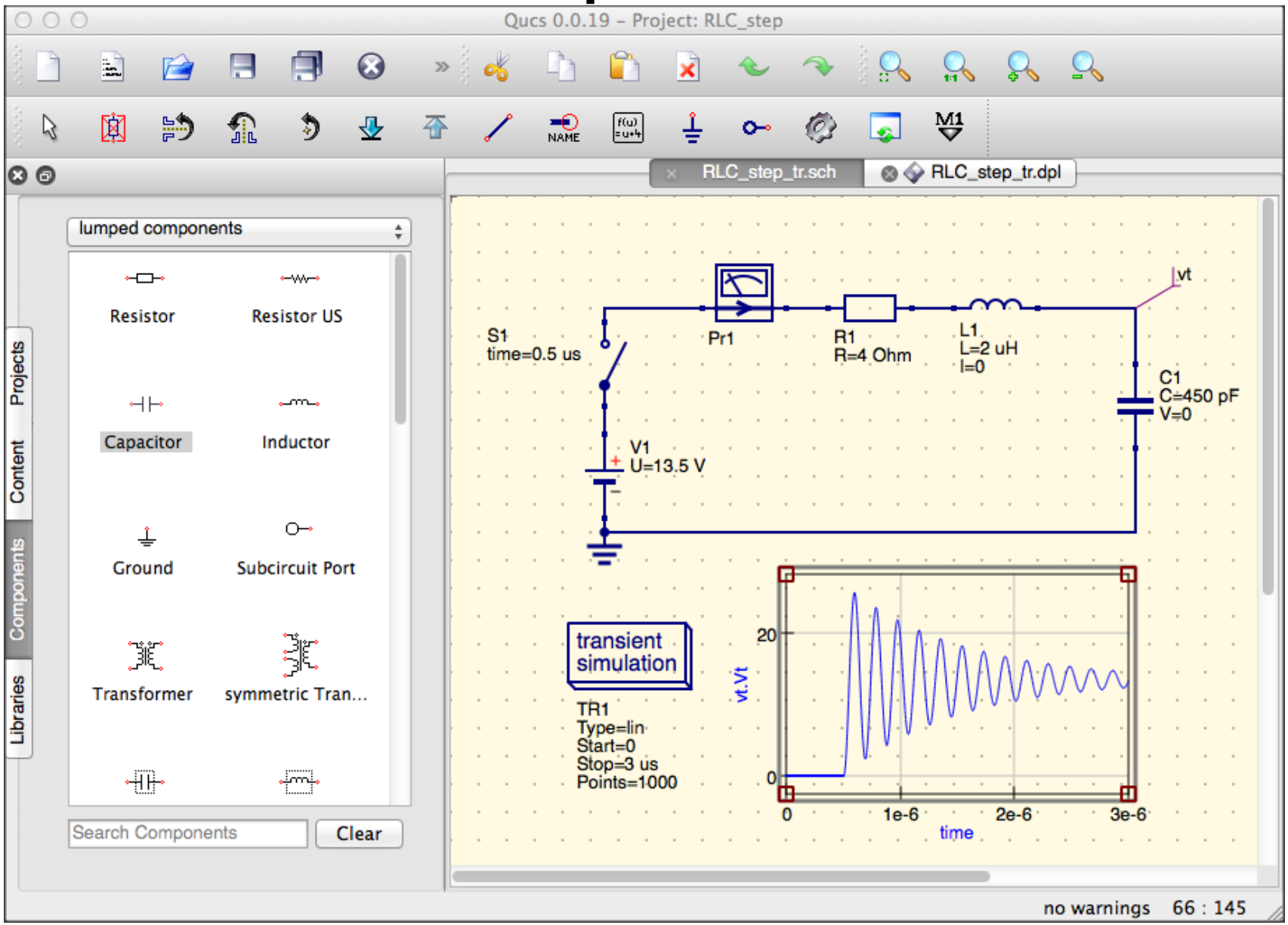
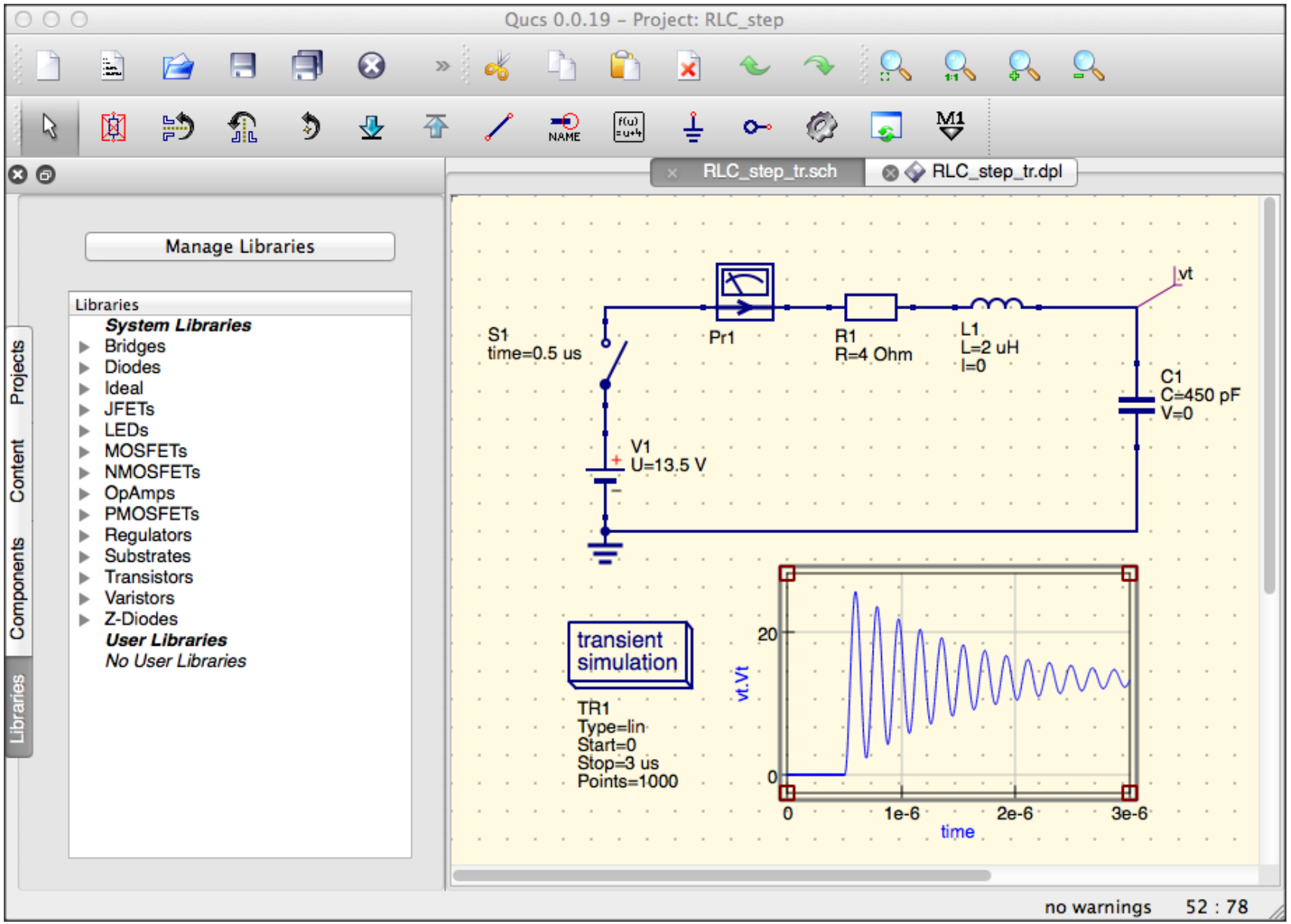
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
65 : 35

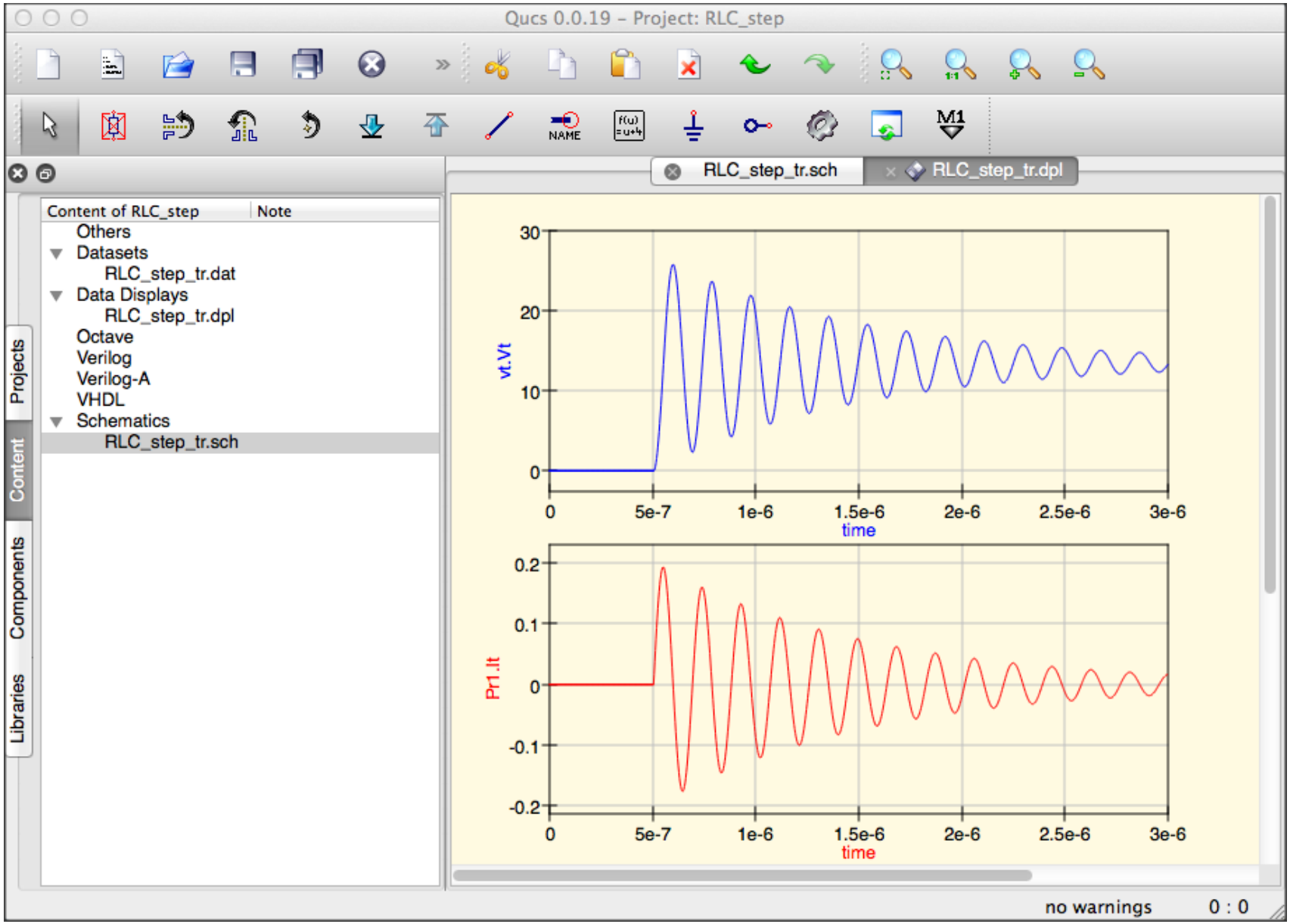
Components


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
lumped components
Resistor
Resistor US
Capacitor
Inductor
Ground
Subcircuit Port
Transformer
symmetric Tran...
Search Components
Clear
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
66 : 145

Libraries


Qucs 0.0.19 – Project: RLC_step
RLC_step_tr.sch
RLC_step_tr.dpl
Manage Libraries
Libraries
System Libraries
Bridges
Diodes
Ideal
JFETs
LEDs
MOSFETs
NMOSFETs
OpAmps
PMOSFETs
Regulators
Substrates
Transistors
Varistors
Z-Diodes
User Libraries
No User Libraries
Projects
Content
Components
Libraries
S1
time=0.5 us
Pr1
R1
R=4 Ohm
L1
L=2 uH
I=0
vt
C1
C=450 pF
V=0
V1
U=13.5 V
transient
simulation
TR1
Type=lin
Start=0
Stop=3 us
Points=1000
vt.Vt
20
0
0
1e-6
2e-6
3e-6
time
no warnings
52 : 78

Visualization



Qucs-ActiveFilter (1)

Filter parameters

Passband attenuation, Ap (dB)	3
Stopband attenuation, As (dB)	20
Cuttof frequency, Fc (Hz)	1000
Stopband frequency, Fs (Hz)	1200
Passband ripple Rp(dB)	3
Passband gain, Kv (dB)	0
Filter order	5

Transfer function and Topology

Approximation type: Butterworth

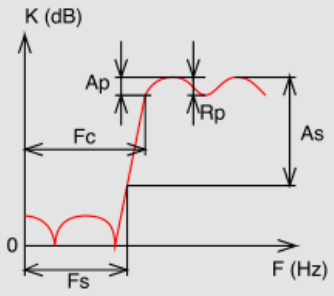
Manually define transfer function

Filter type: High Pass

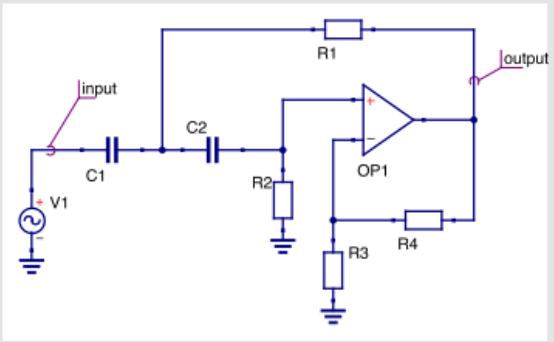
Filter topology: Sallen-Key (S-K)

Calculate and copy to clipboard

General filter amplidure-frequency response



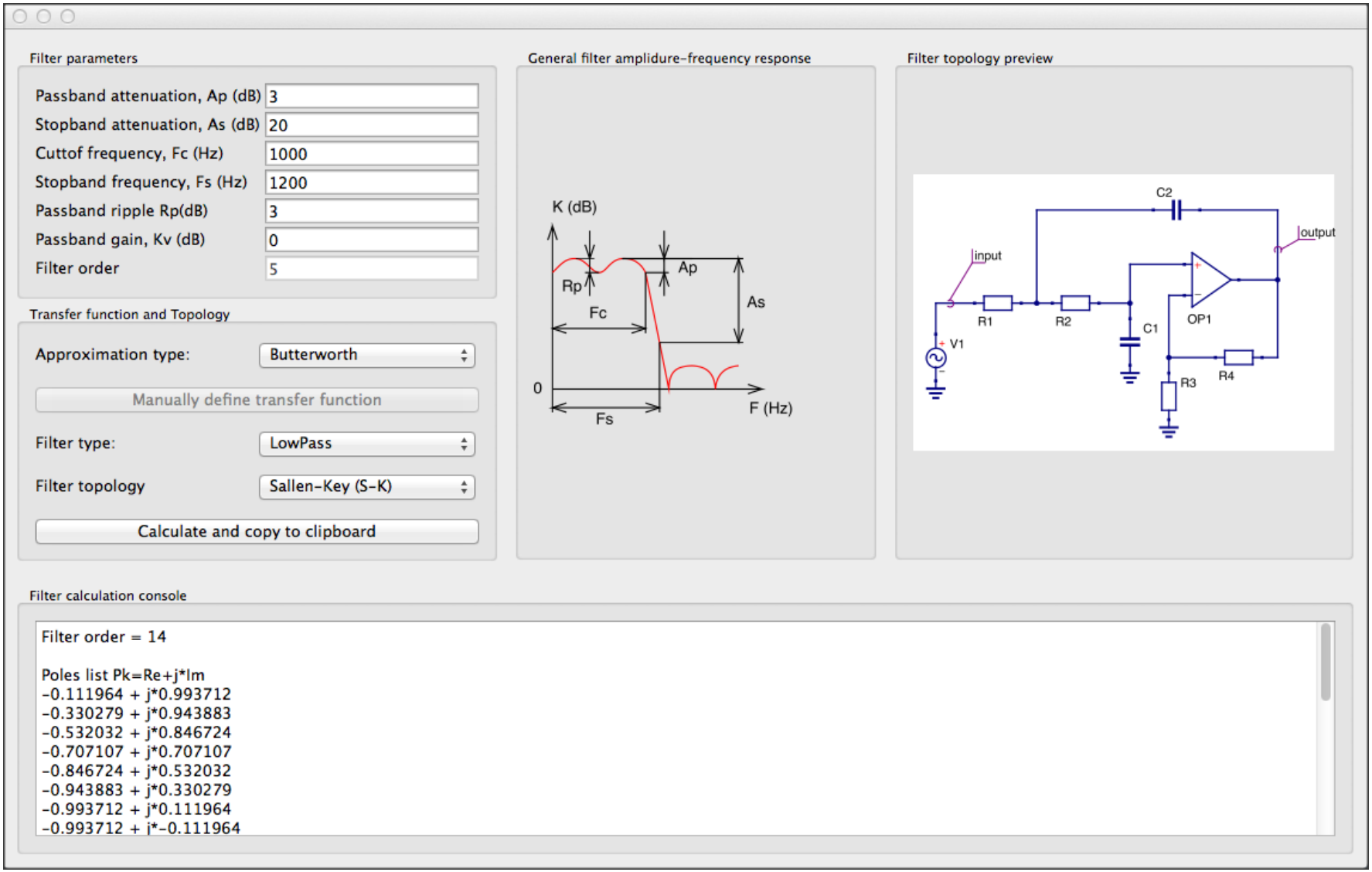
Filter topology preview



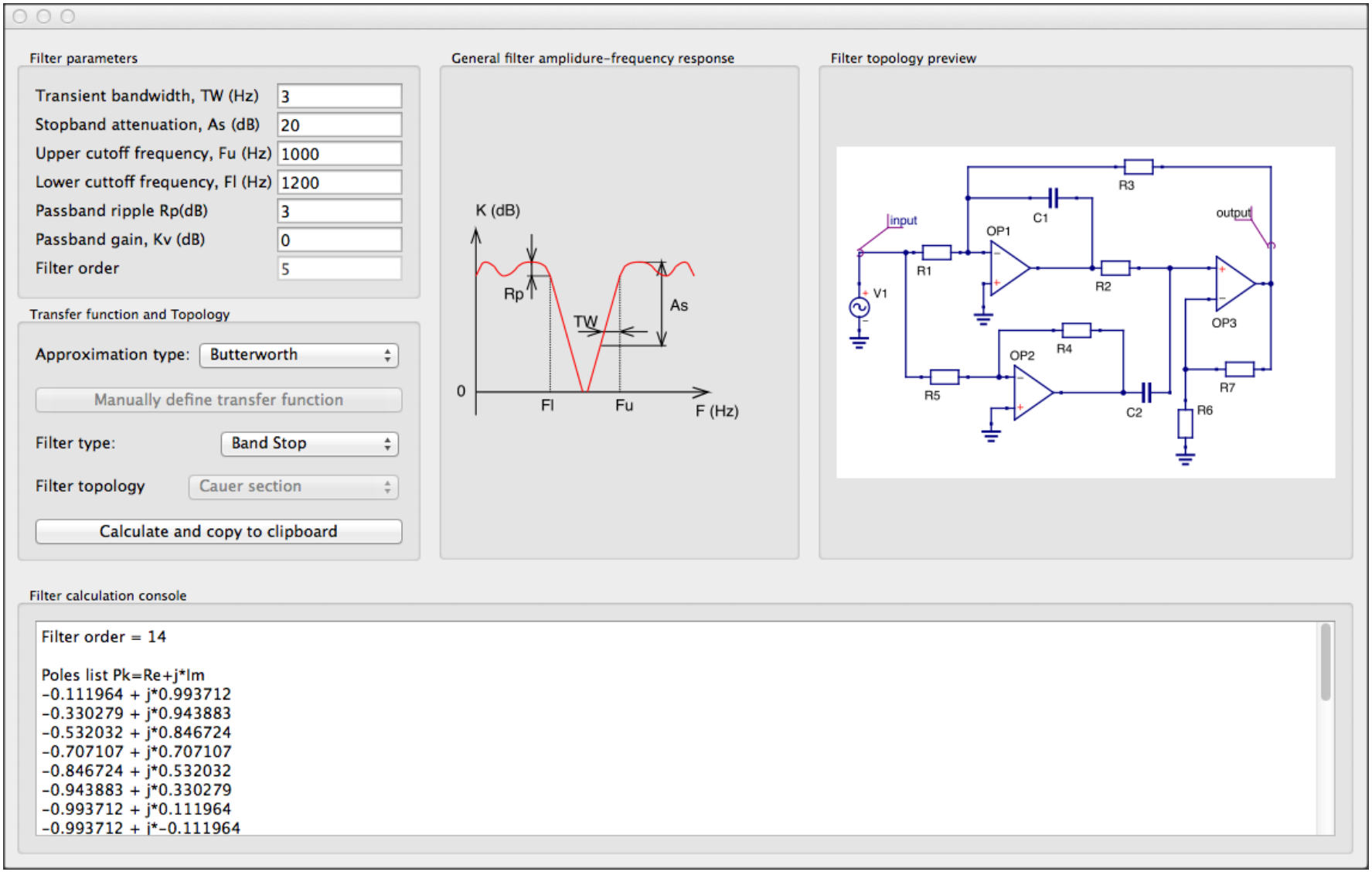
Filter calculation console

```
Filter order = 14

Poles list Pk=Re+j*Im
-0.111964 + j*0.993712
-0.330279 + j*0.943883
-0.532032 + j*0.846724
-0.707107 + j*0.707107
-0.846724 + j*0.532032
-0.943883 + j*0.330279
-0.993712 + j*0.111964
-0.993712 + j*-0.111964
```

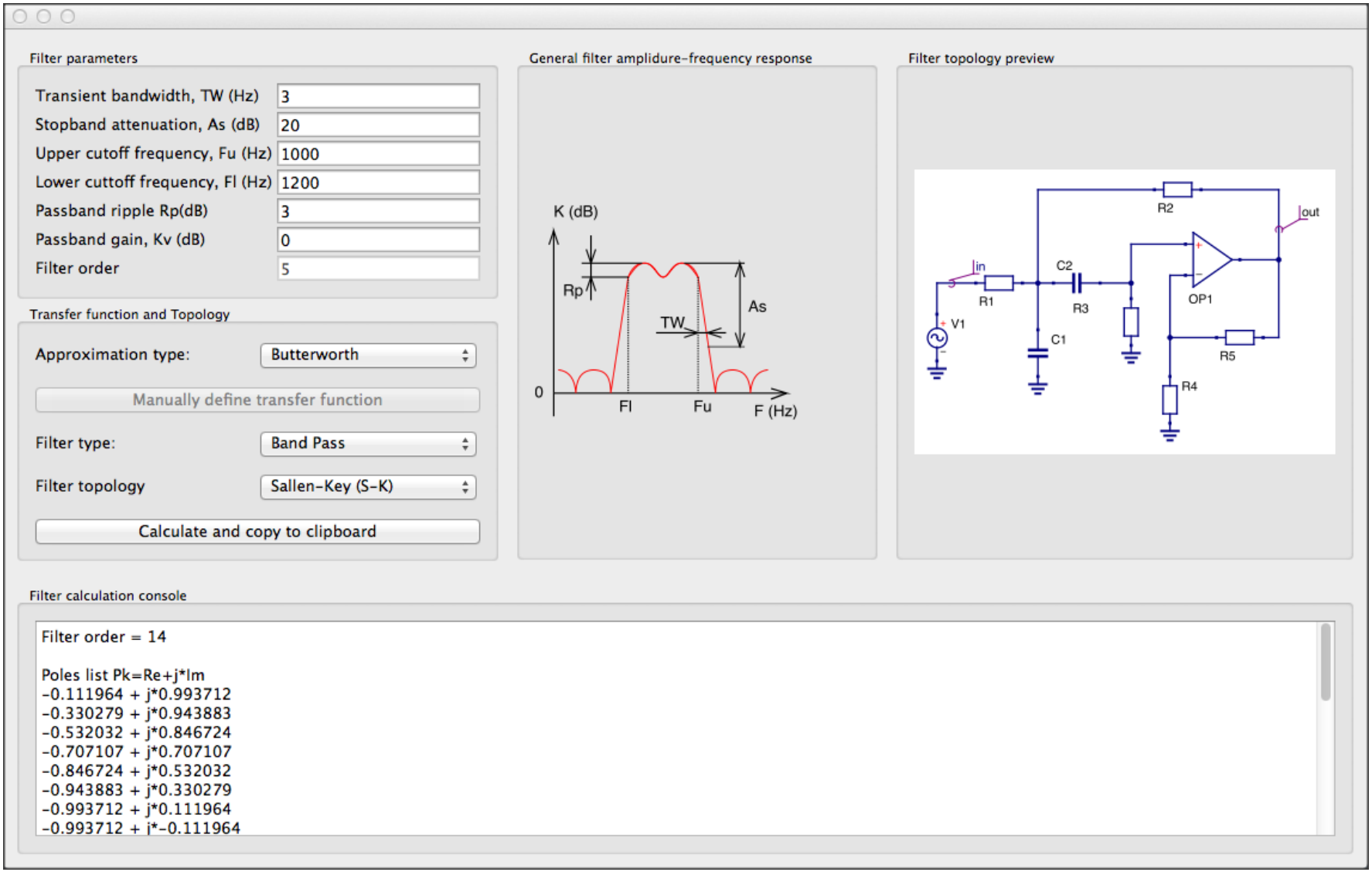
Qucs-ActiveFilter (2)



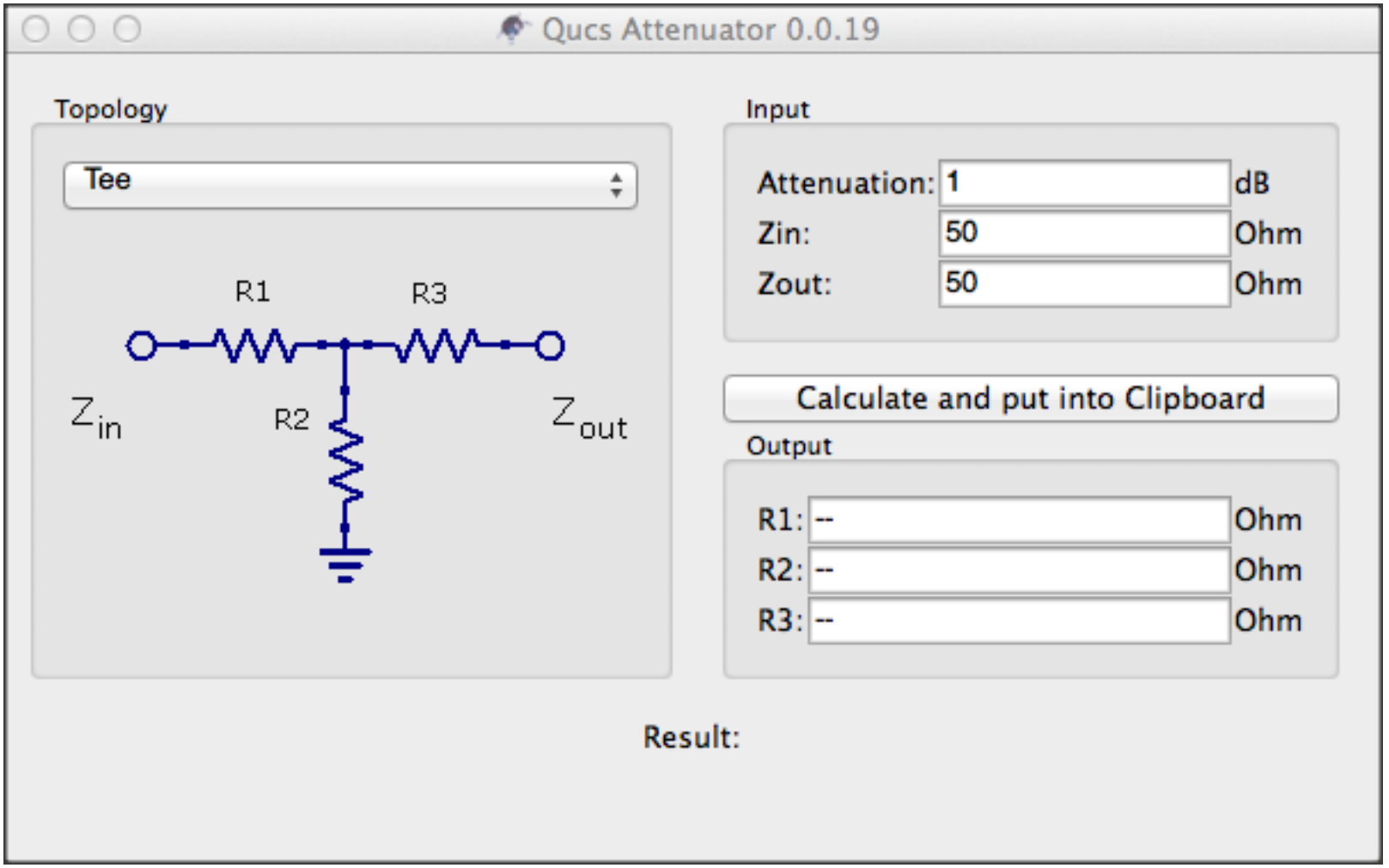
Qucs-ActiveFilter (3)



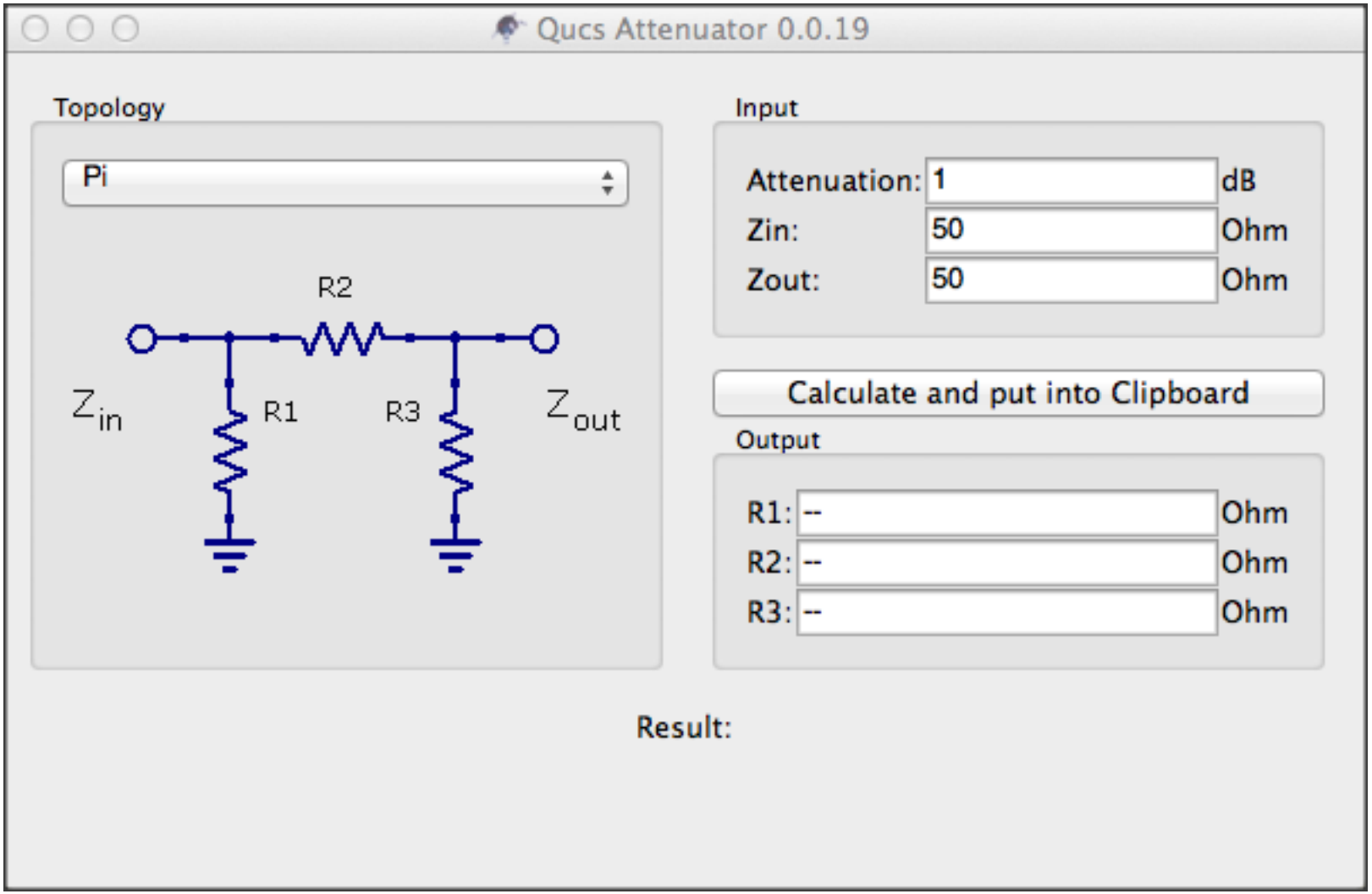
Qucs-ActiveFilter (4)



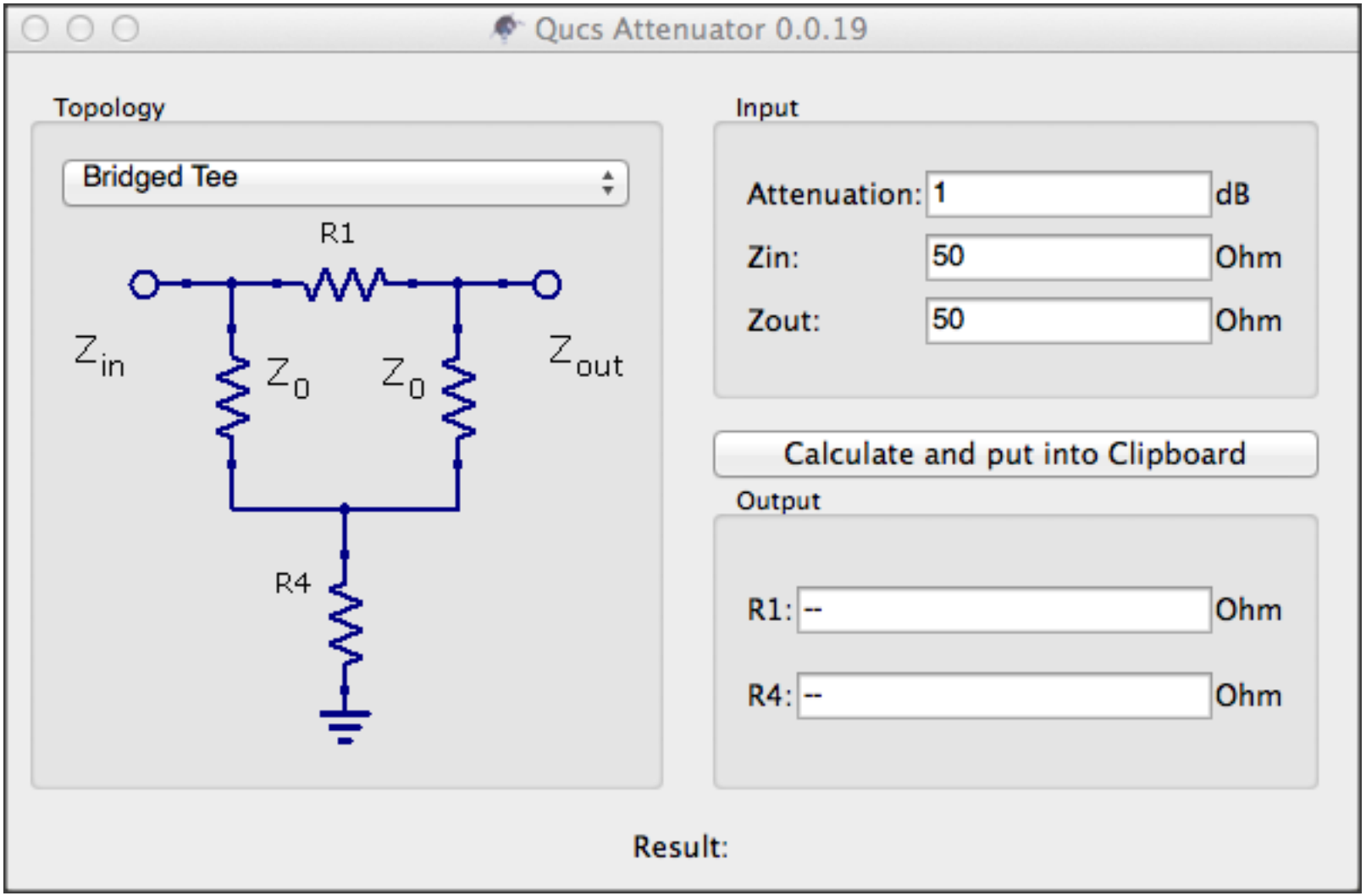
Qucs-Attenuator (1)



Qucs-Attenuator (2)



Qucs-Attenuator (3)



Qucs-Help

Qucs Help System

Contents

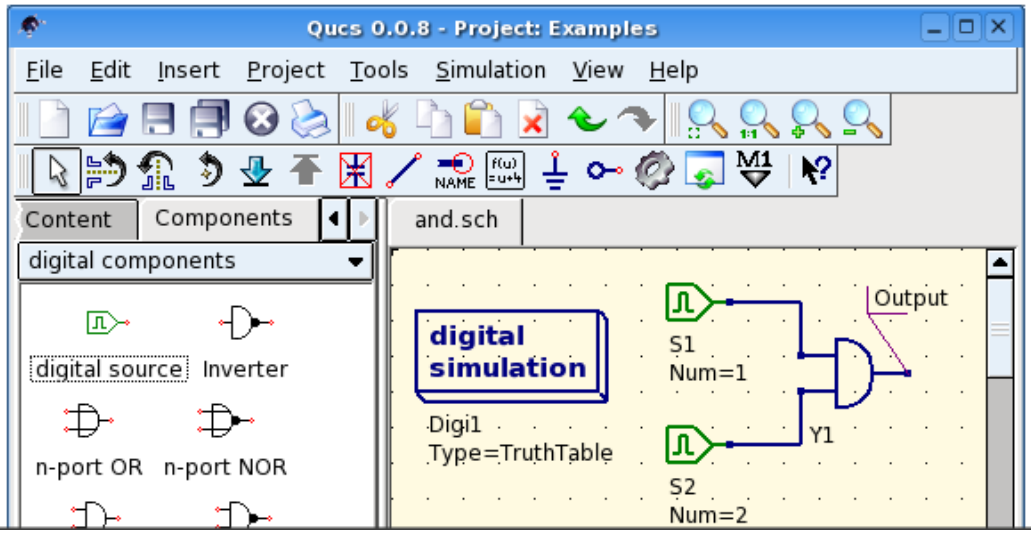
- Home
- Getting Started – Analog Simulation
- Getting Started – Digital Simulation
- Getting Started – Optimization
- Getting Started – Octave Scripts
- Short Description of Actions
- Working with Subcircuits
- Short Description of mathematical Functior
- List of Special Characters
- Creating Matching Circuits
- Description of the installed Qucs files

Getting Started with Digital Simulations

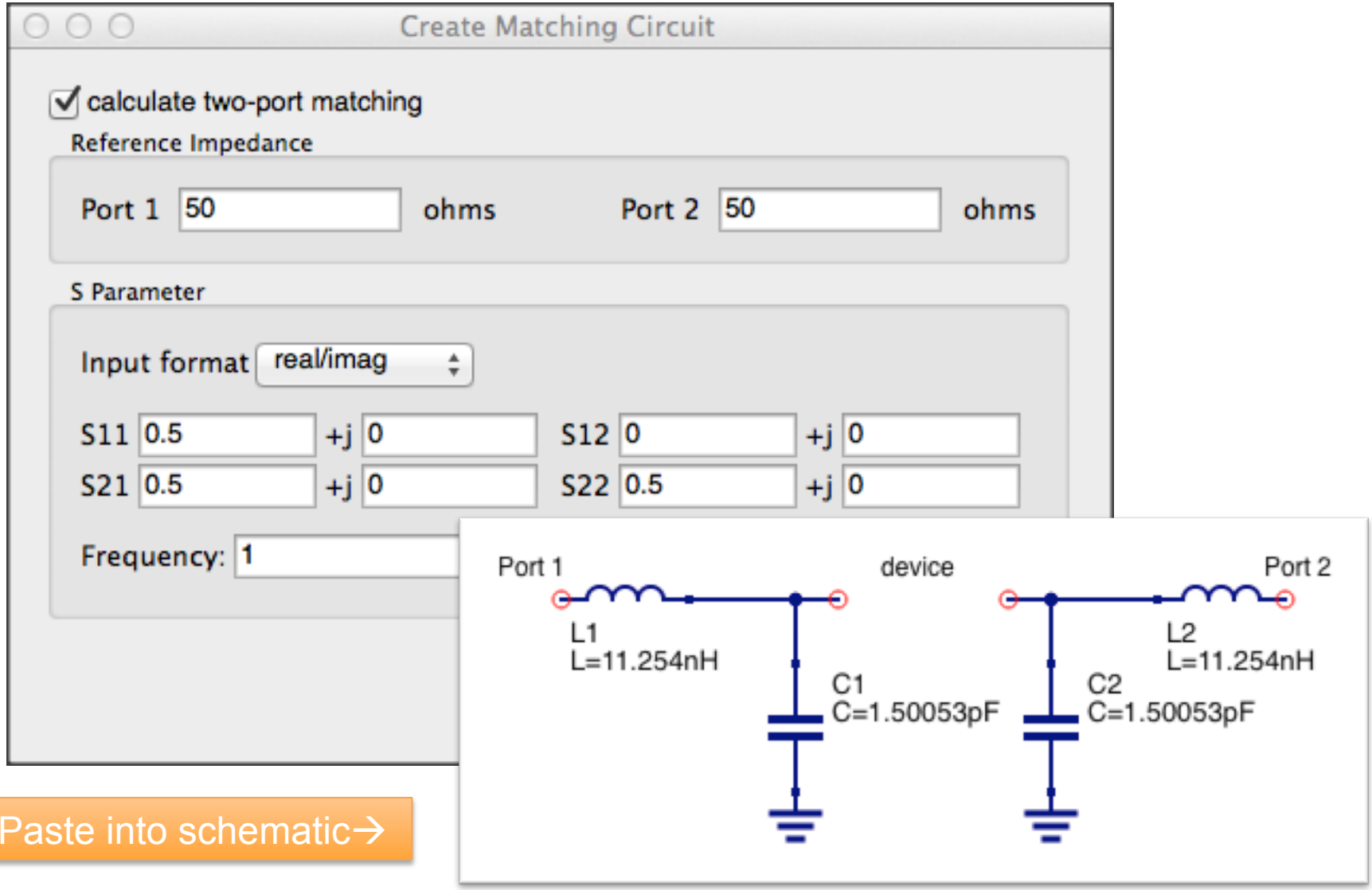
Qucs is also a graphical user interface for performing digital simulations. This document should give you a short description on how to use it.

For digital simulations Qucs uses the FreeHDL program (http://www.freehdl.seul.org). So the FreeHDL package as well as the GNU C++ compiler must be installed on the computer.

There is no big difference in running an analog or a digital simulation. So having read the Getting Started for analog simulations, it is now easy to get a digital simulation work. Let us compute the truth table of a simple logical AND cell. Select the digital components in the combobox of the components tab on the left-hand side and build the circuit shown in figure 1. The digital simulation block can be found among the other simulation blocks. The digital sources *S1* and *S2* are the inputs, the node labeled as *Output* is the output. After performing the simulation, the data display page opens. Place the diagram *truth table* on it and insert the variable *Output*. Now the truth table of a two-port AND cell is shown. Congratulation, the first digital simulation is done!

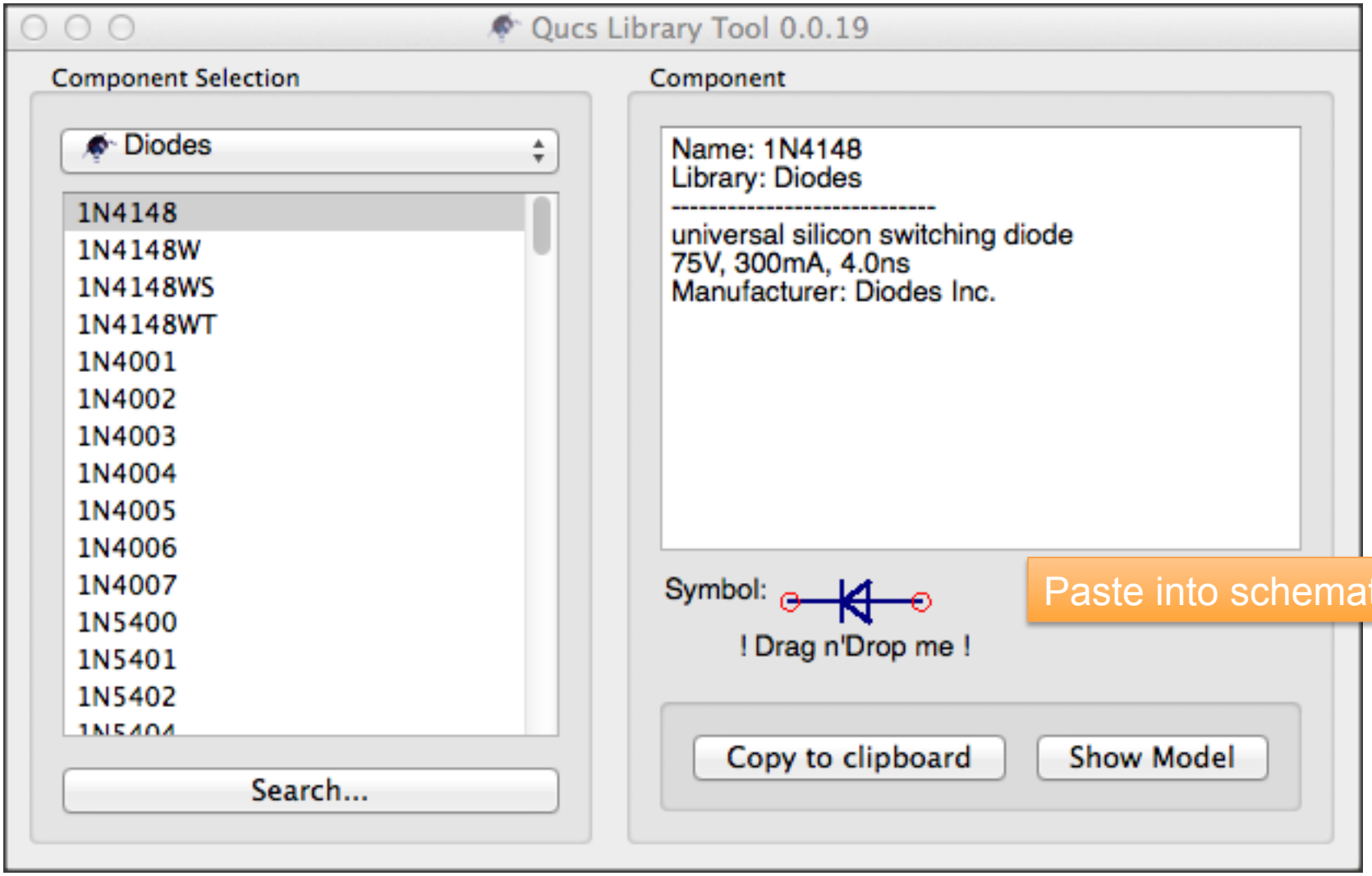


Qucs-Matching

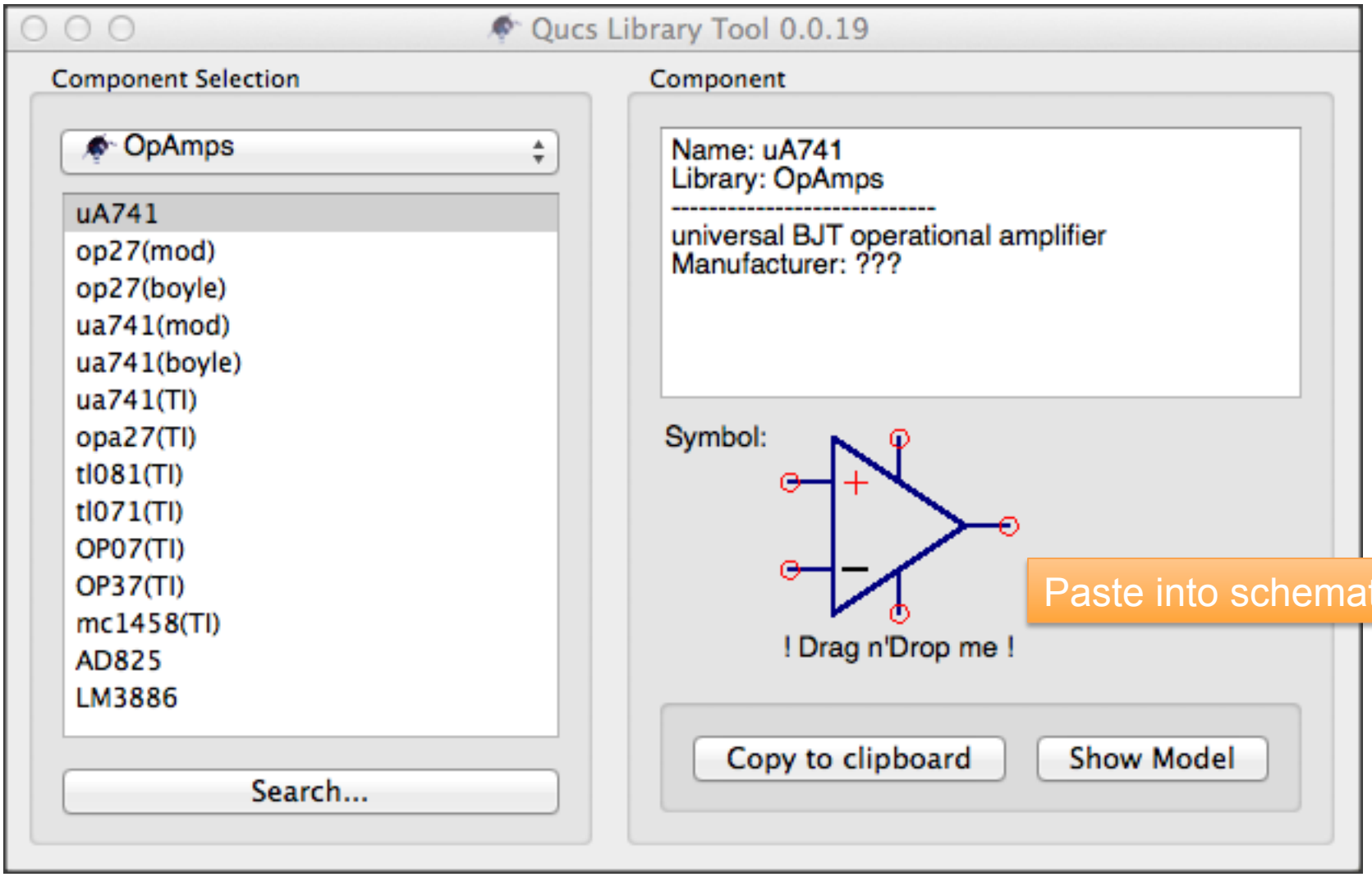


Paste into schematic→

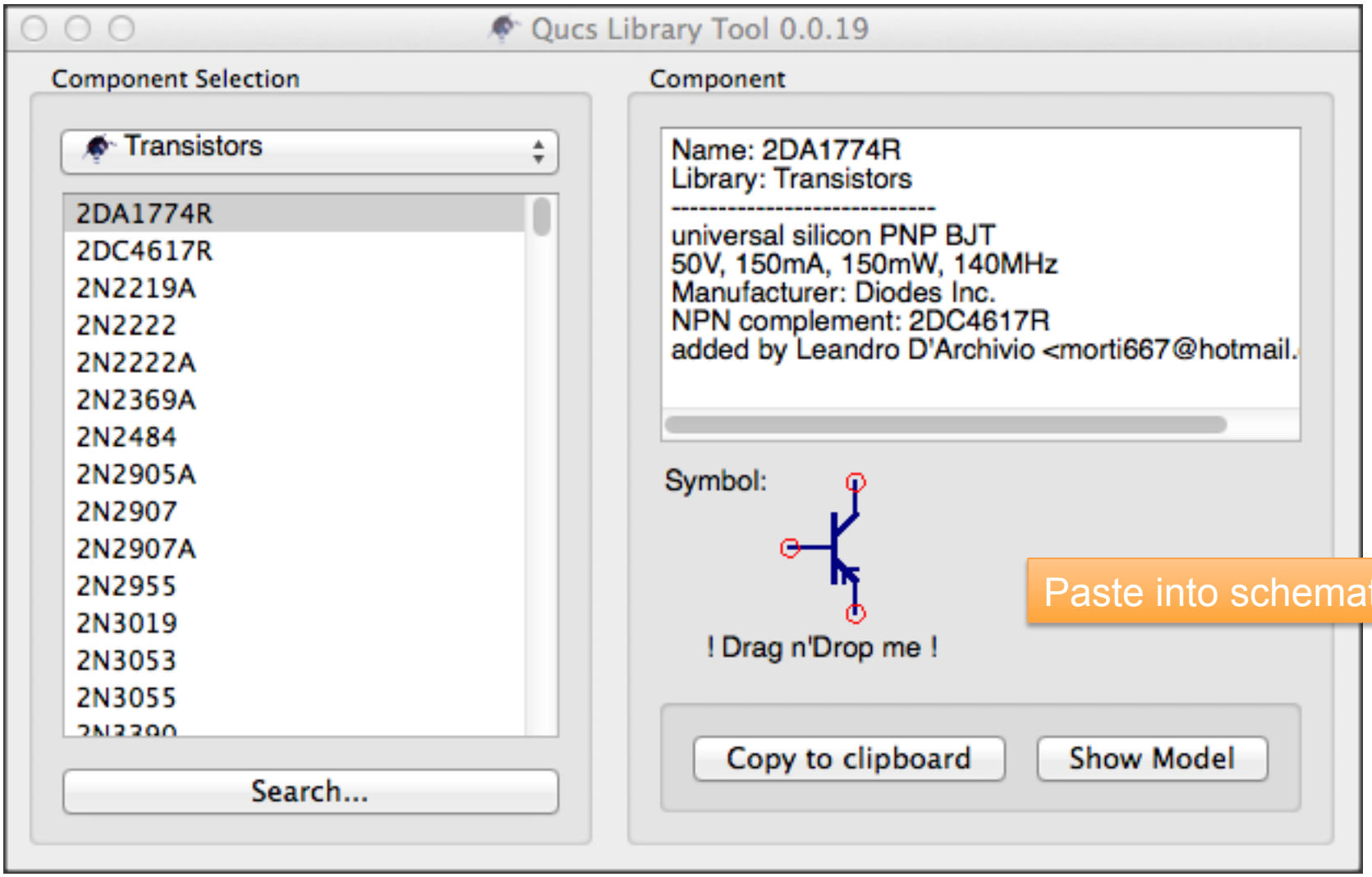
Qucs-Lib (1)


Qucs Library Tool 0.0.19
Component Selection
Diodes
1N4148
1N4148W
1N4148WS
1N4148WT
1N4001
1N4002
1N4003
1N4004
1N4005
1N4006
1N4007
1N5400
1N5401
1N5402
Search...
Component
Name: 1N4148
Library: Diodes
universal silicon switching diode
75V, 300mA, 4.0ns
Manufacturer: Diodes Inc.
Symbol:
! Drag n'Drop me !
Paste into schematic→
Copy to clipboard
Show Model

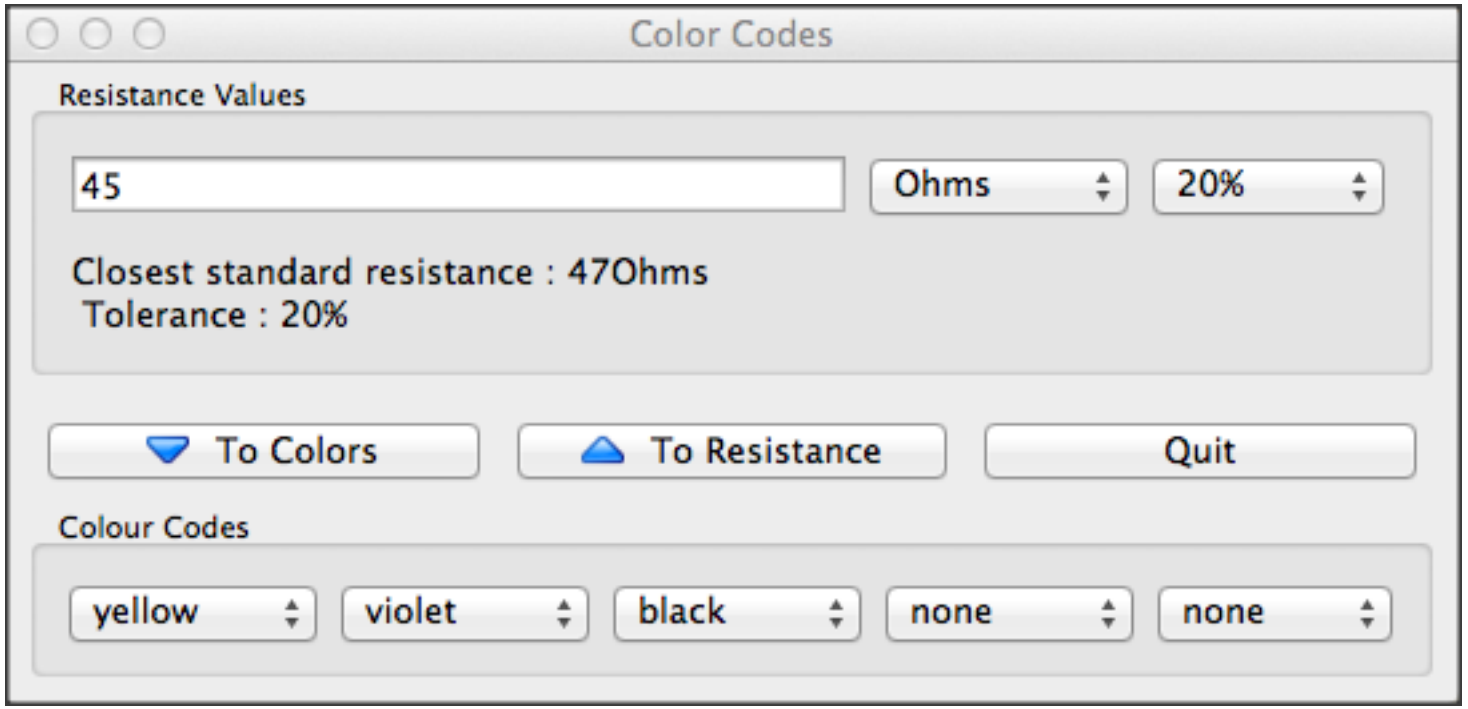
Qucs-Lib (2)


Qucs Library Tool 0.0.19
Component Selection
OpAmps
uA741
op27(mod)
op27(boyle)
ua741(mod)
ua741(boyle)
ua741(TI)
opa27(TI)
tl081(TI)
tl071(TI)
OP07(TI)
OP37(TI)
mc1458(TI)
AD825
LM3886
Search...
Component
Name: uA741
Library: OpAmps
universal BJT operational amplifier
Manufacturer: ???
Symbol:
! Drag n'Drop me !
Paste into schematic→
Copy to clipboard
Show Model

Qucs-Lib (3)

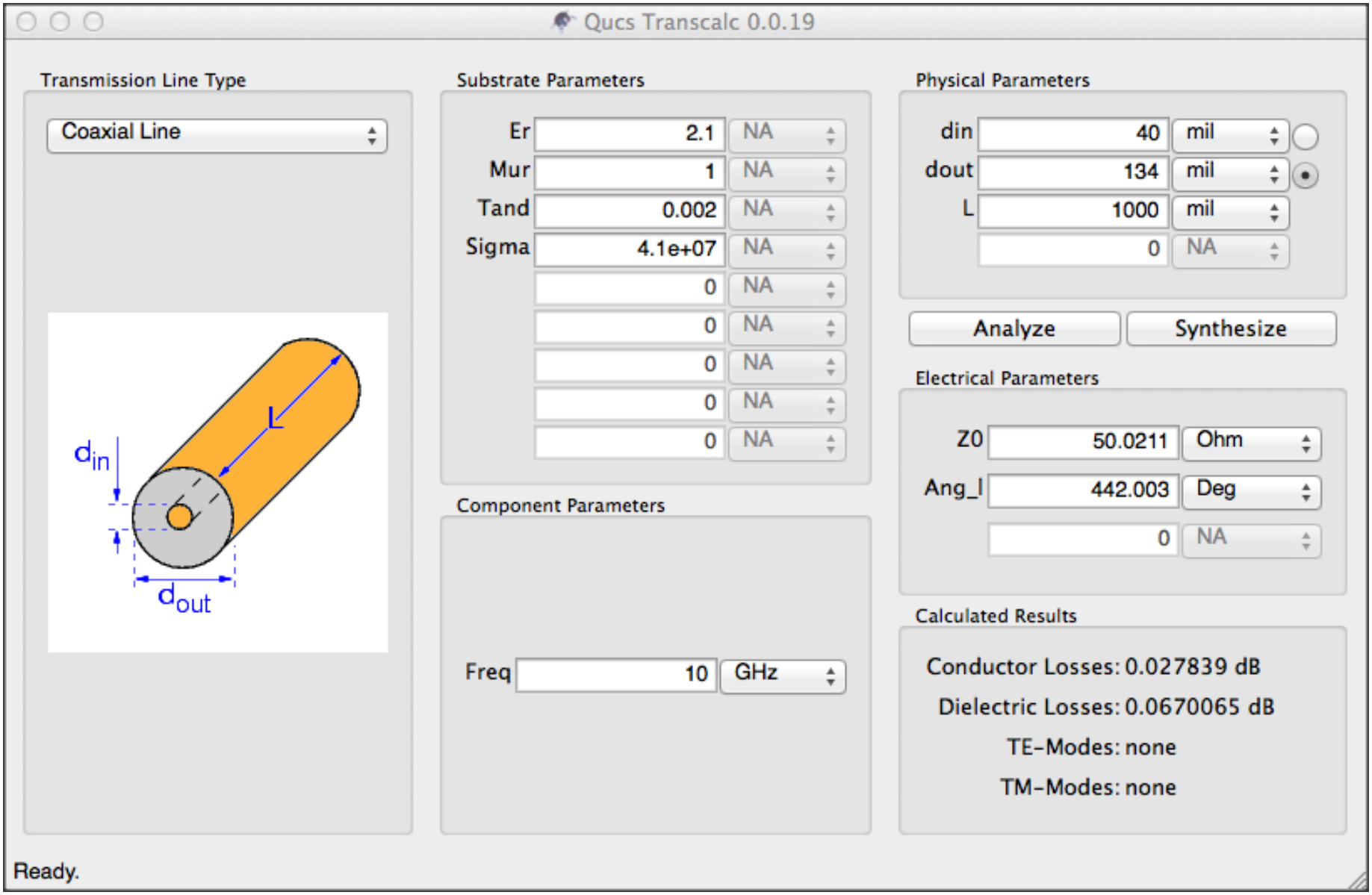

Qucs Library Tool 0.0.19
Component Selection
Transistors
2DA1774R
2DC4617R
2N2219A
2N2222
2N2222A
2N2369A
2N2484
2N2905A
2N2907
2N2907A
2N2955
2N3019
2N3053
2N3055
Search...
Component
Name: 2DA1774R
Library: Transistors
universal silicon PNP BJT
50V, 150mA, 150mW, 140MHz
Manufacturer: Diodes Inc.
NPN complement: 2DC4617R
added by Leandro D'Archivio <morti667@hotmail.
Symbol:
! Drag n'Drop me !
Copy to clipboard
Show Model
Paste into schematic→

Qucs-Rescodes

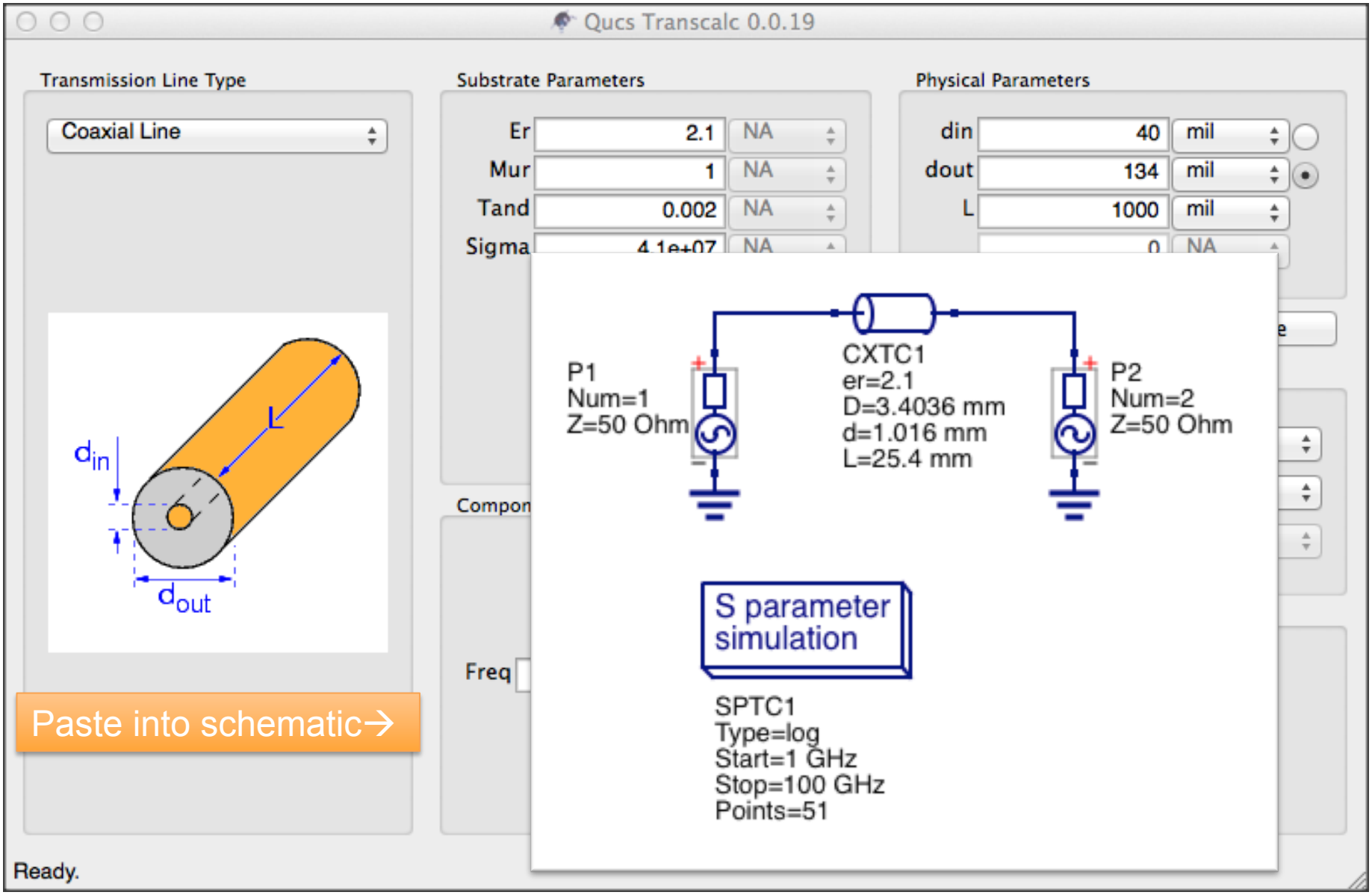


Paste into schematic→

Qucs-Transcalc (1)



Qucs-Transcalc (2)



Qucs-Transcalc (3)

Qucs Transcalc 0.0.19

Transmission Line Type

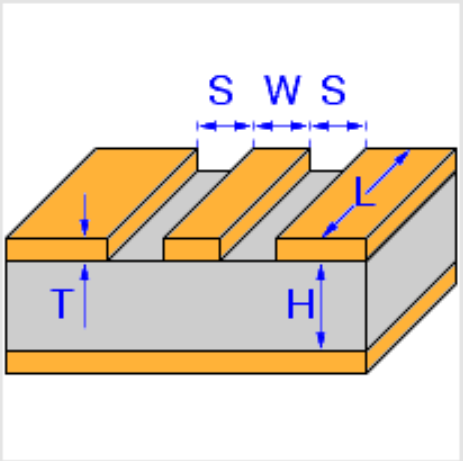
Grounded Coplanar

Substrate Parameters

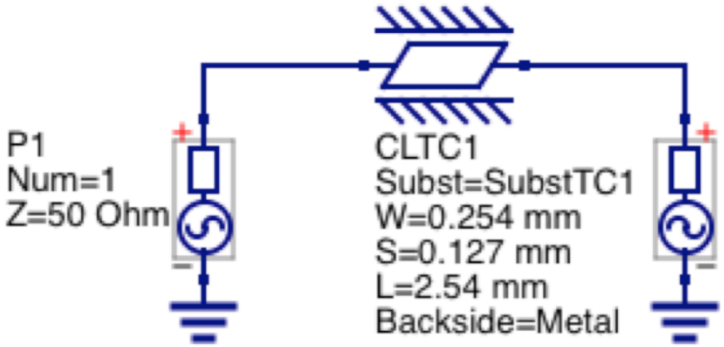
Er	2.94	NA
H	10	mil
T	0.1	mil

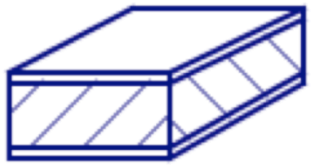
Physical Parameters

W	10	mil
S	5	mil
L	100	mil



Paste into schematic→





SubstTC1
er=2.94
h=0.254 mm
t=2.54 um
tand=0
rho=2.43902e-08
D=0

S parameter simulation

SPTC1
Type=log
Start=0.1 GHz
Stop=10 GHz
Points=51

Equation

EqnTC1
A=twoport(S,'S','A')
ZL=real(sqrt(A[1,2]/A[2,1]))

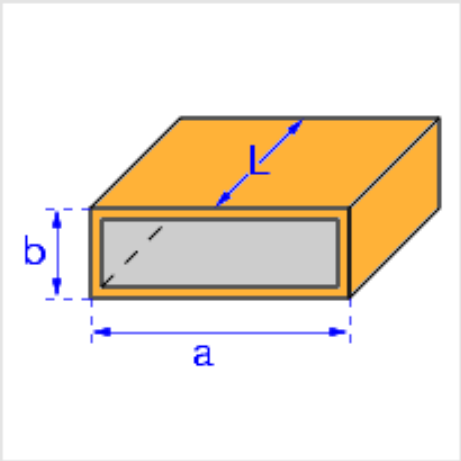
Ready.

Qucs-Transcalc (4)

Qucs Transcalc 0.0.19

Transmission Line Type

Rectangular Waveguide

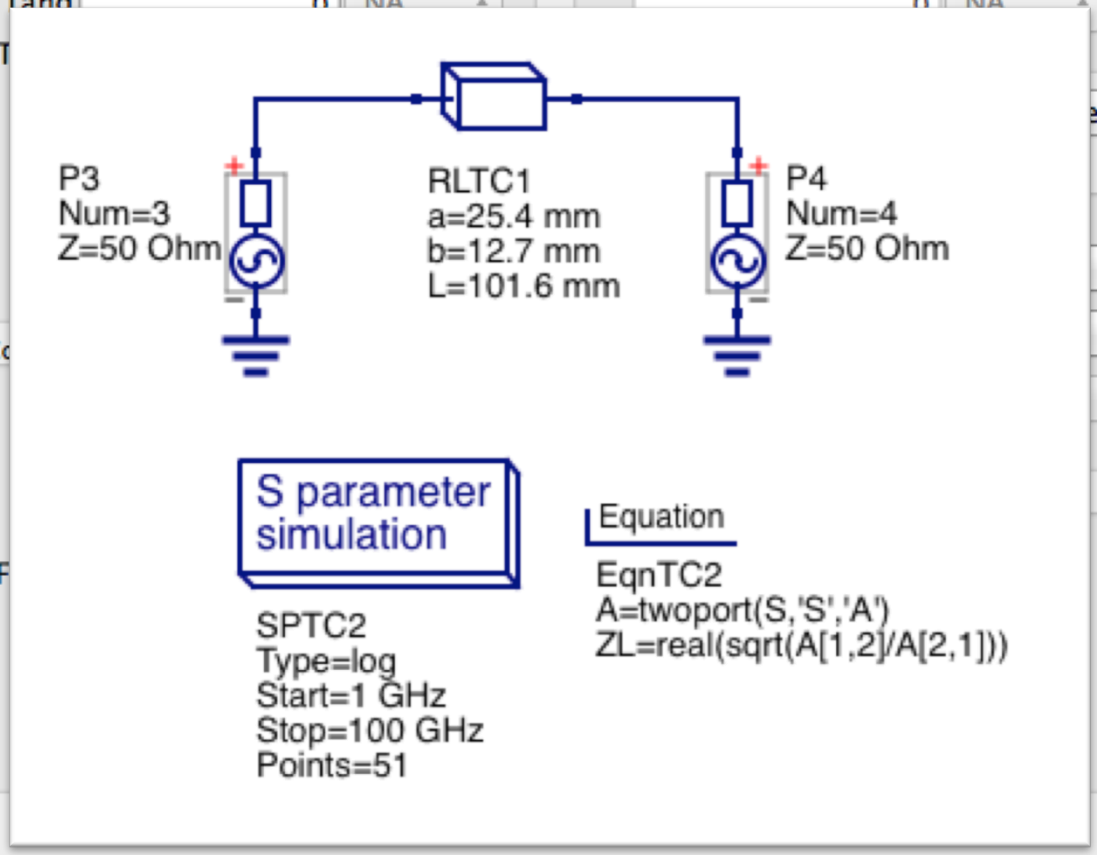


Substrate Parameters

Er	1	NA
Mur	1	NA
Cond	4.1e+07	NA
Tand	0	NA

Physical Parameters

a	1000	mil
b	500	mil
L	4000	mil



Paste into schematic→

Ready.

Qucs-Transcalc (5)

Qucs Transcalc 0.0.19

Transmission Line Type

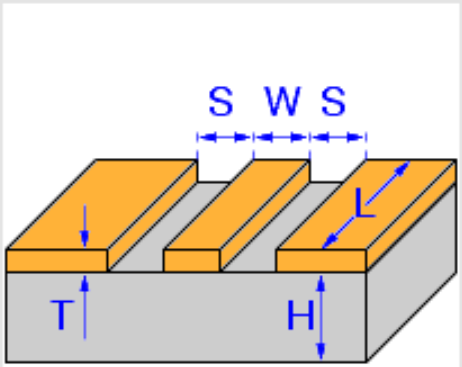
Coplanar Waveguide

Substrate Parameters

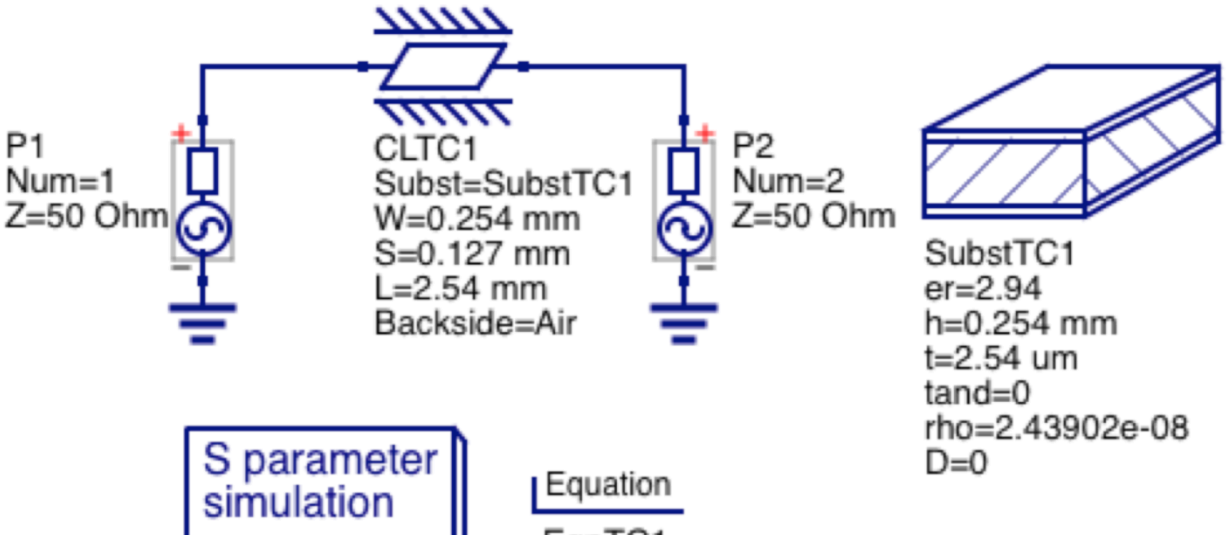
Er	2.94	NA
H	10	mil
T	0.1	mil

Physical Parameters

W	10	mil
S	5	mil
L	100	mil



Paste into schematic→



Ready.

Qucs-Transcalc (6)

Qucs Transcalc 0.0.19

Transmission Line Type

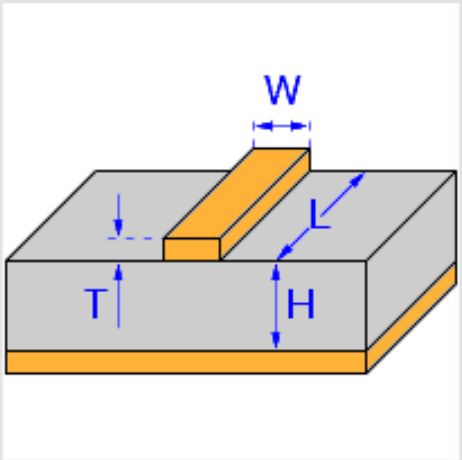
Microstrip Line

Substrate Parameters

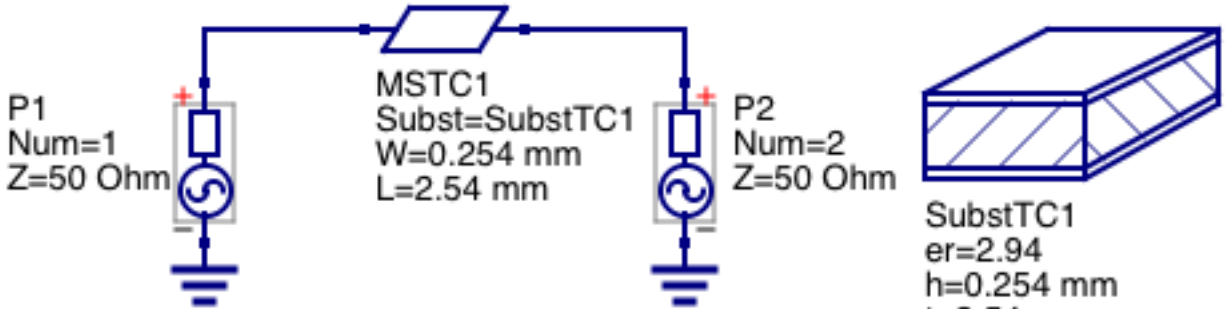
Er	2.94	NA
Mur	1	NA
H	10	mil
H_t	1e+20	mil

Physical Parameters

W	9.99999	mil
L	99.9999	mil
	0	NA
	0	NA



Paste into schematic→



S parameter simulation

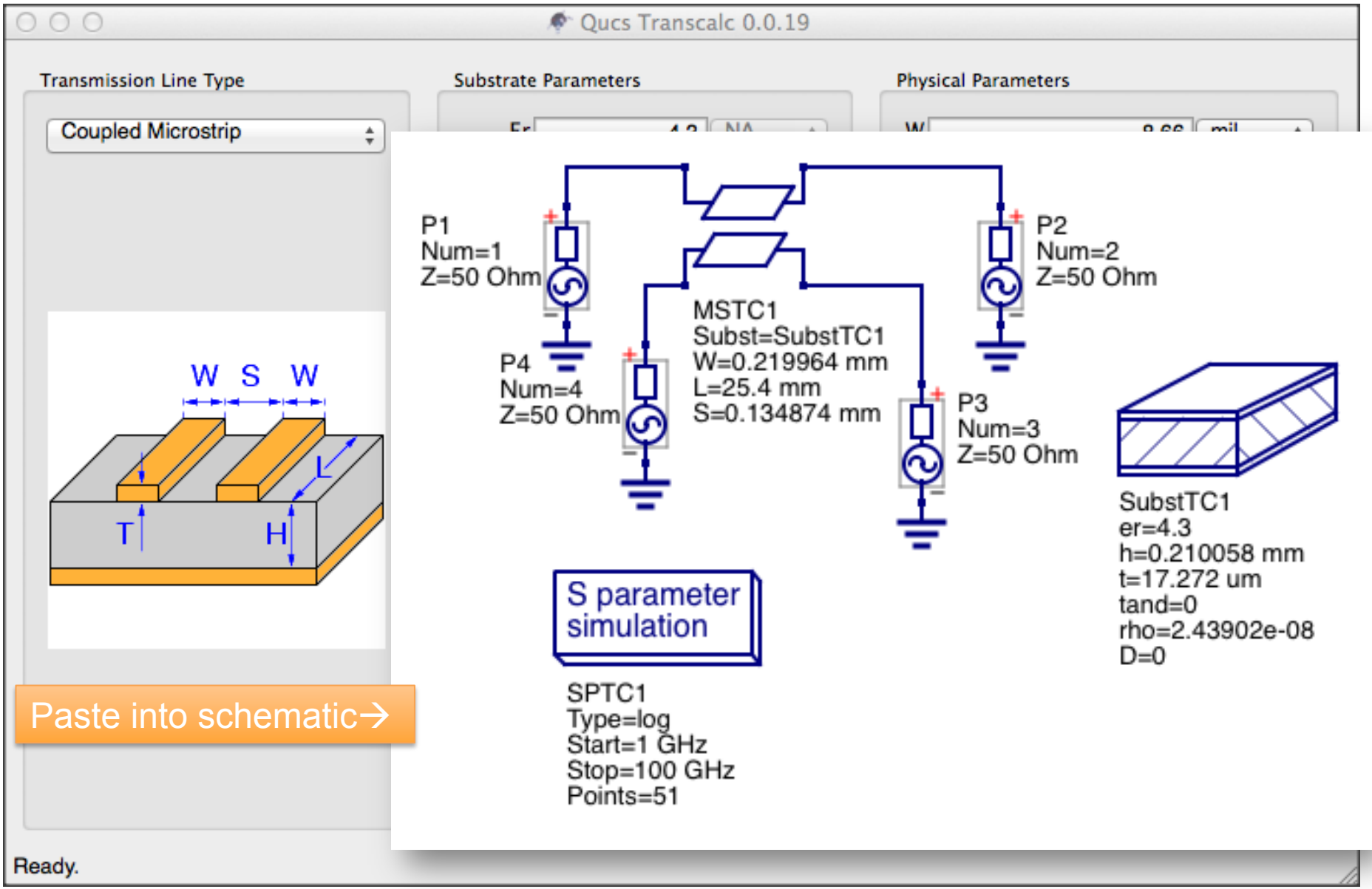
SPTC1
Type=log
Start=0.1 GHz
Stop=10 GHz
Points=51

Equation

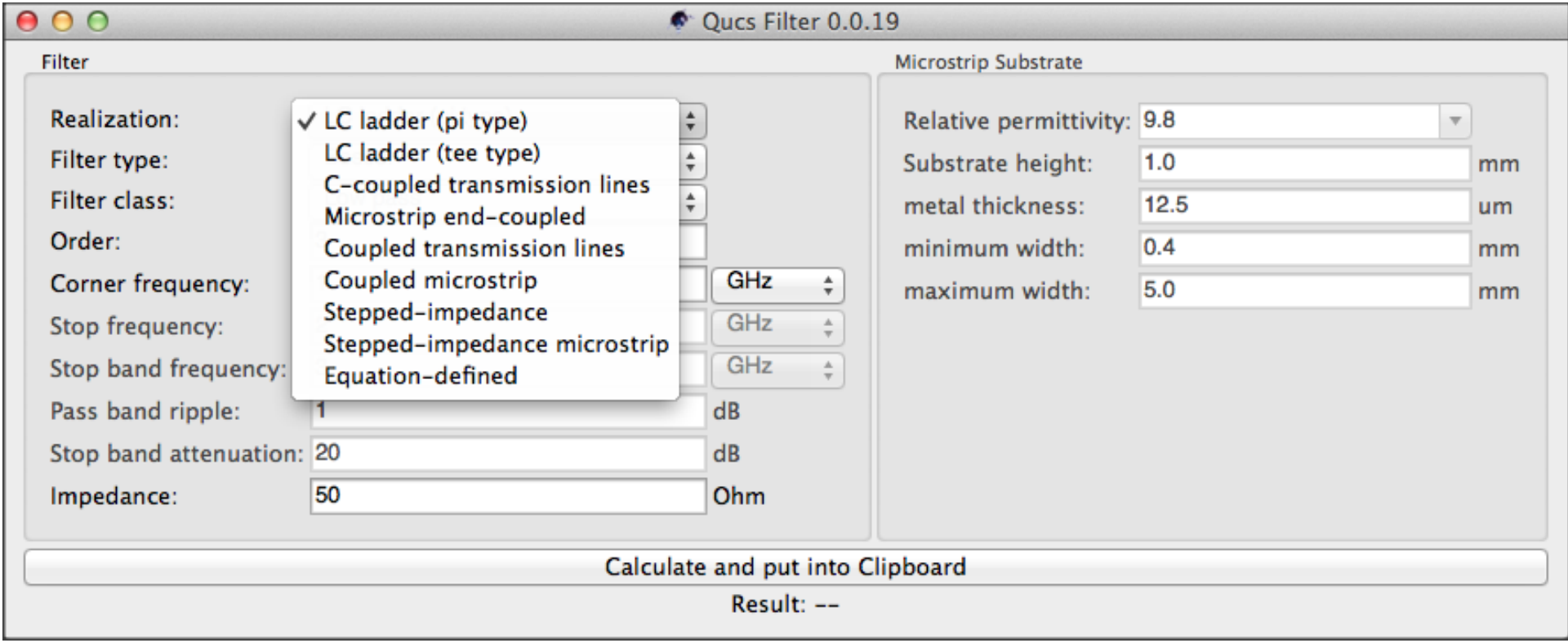
EqnTC1
A=twoport(S,'S','A')
ZL=real(sqrt(A[1,2]/A[2,1]))

Ready.

Qucs-Transcalc



Qucs-Filter



Paste into schematic→

Command Line Tools

- Qucs – schematic
  - schematic to netlist
  - schematic to print
  - dump components data
- Qucsator – simulator
  - DC
  - Transient
  - AC
  - AC Noise
  - S-Parameter
  - S-Parameter Noise
  - (Harmonic Balance)

- Qucsconv - converter

```
spice       - qucs
spice       - qucslib
vcd         - qucsdata
qucsdata    - csv
qucsdata    - touchstone
citi        - qucsdata
touchstone  - qucsdata
csv         - qucsdata
zvr         - qucsdata
mdl         - qucsdata
qucsdata    - matlab
```

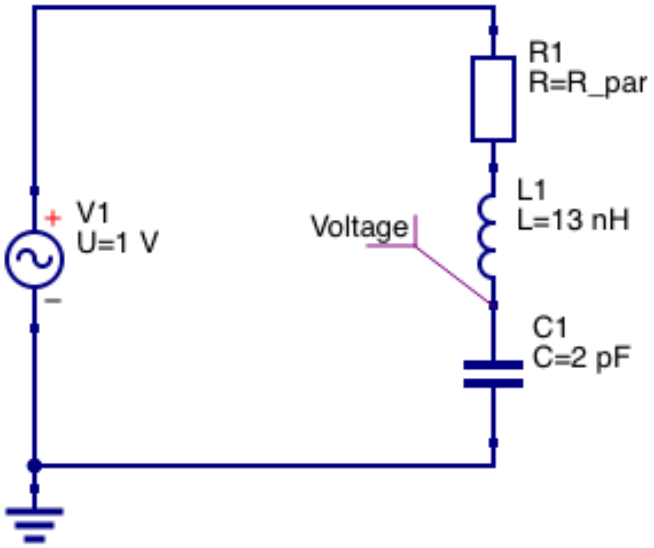
- Custom file formats
  - schematic
  - library
  - netlist
  - data file

Demo

- Examples
  - RLC circuit, parameter sweep
  - 555 timer: macro modeling
  - Optimization: Band-pass filter
  - 10 GHz microstrip band-pass filter
  - Verilog counter

- Development
  - Verilog-A support / model builder
  - Ngspice / Xyce front-end

RLC, parameter sweep



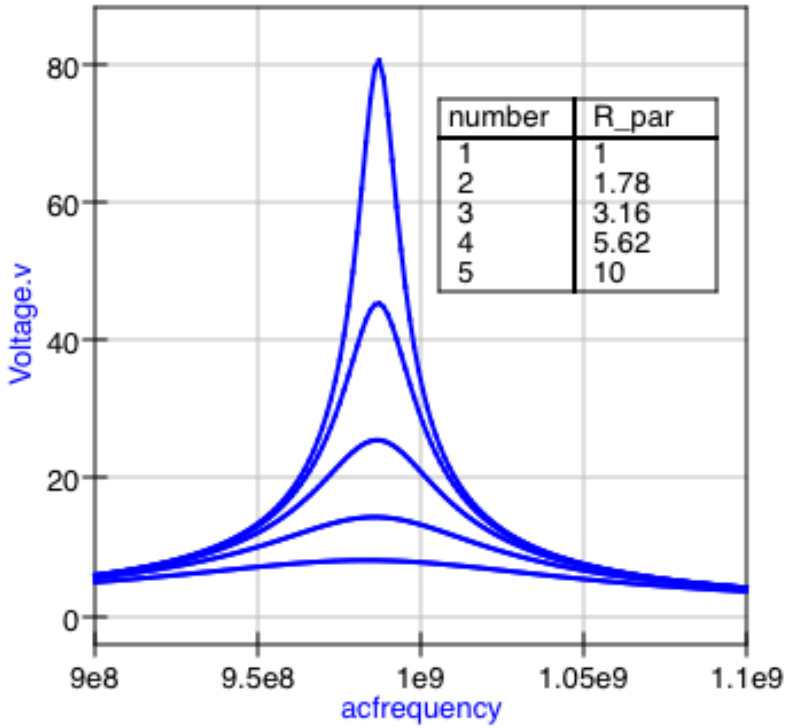
The voltage overshot strongly depends on the quality of the resonance circuit.

ac simulation

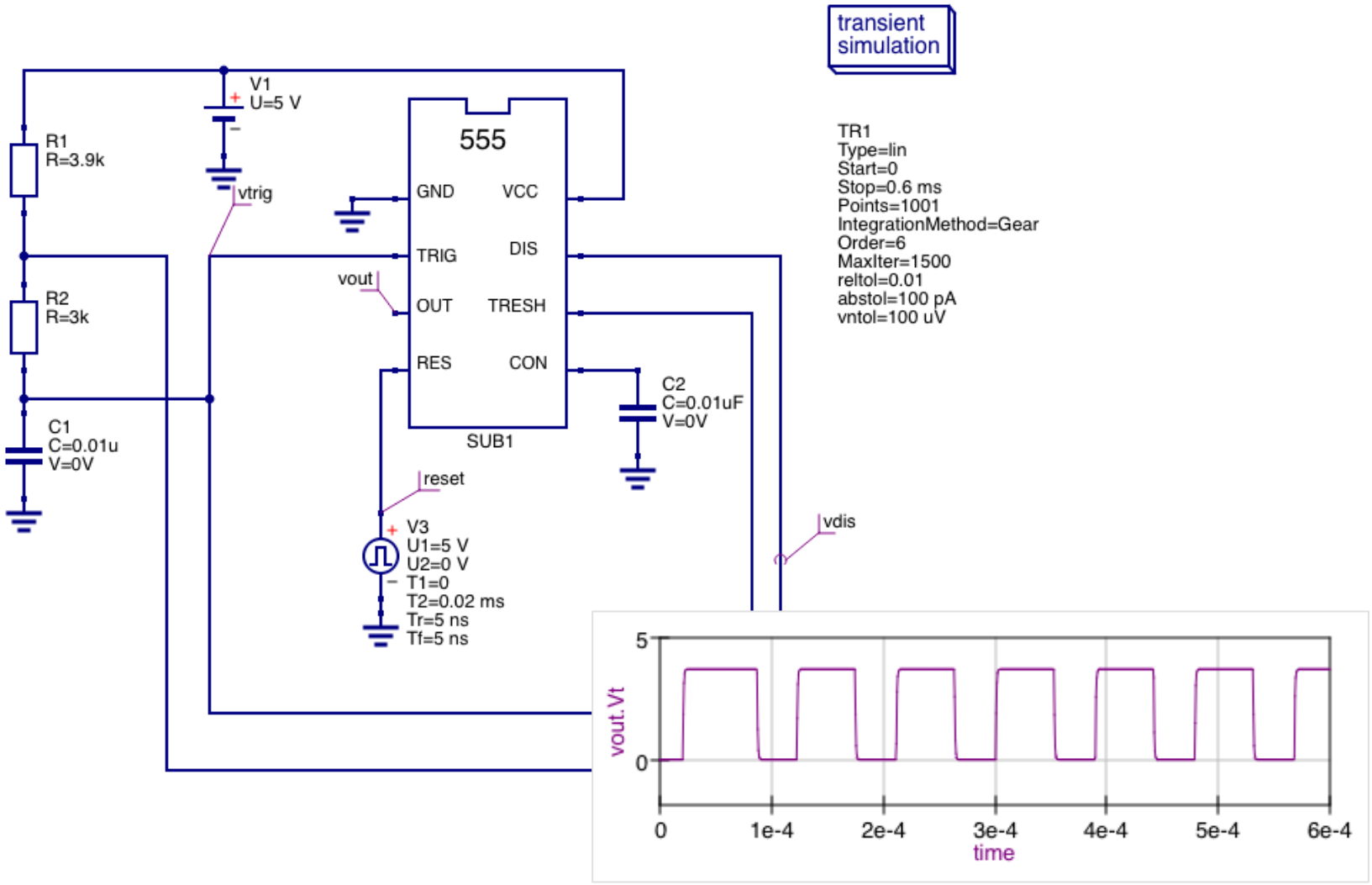
AC1
Type=lin
Start=0.9 GHz
Stop=1.1 GHz
Points=150

Parameter sweep

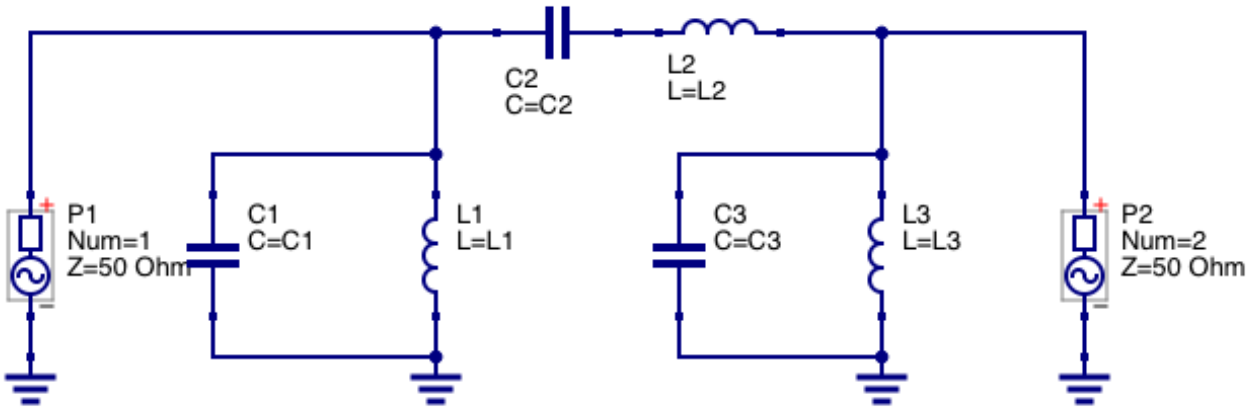
SW1
Sim=AC1
Type=log
Param=R_par
Start=1 Ohm
Stop=10 Ohm
Points=5



555 macro model

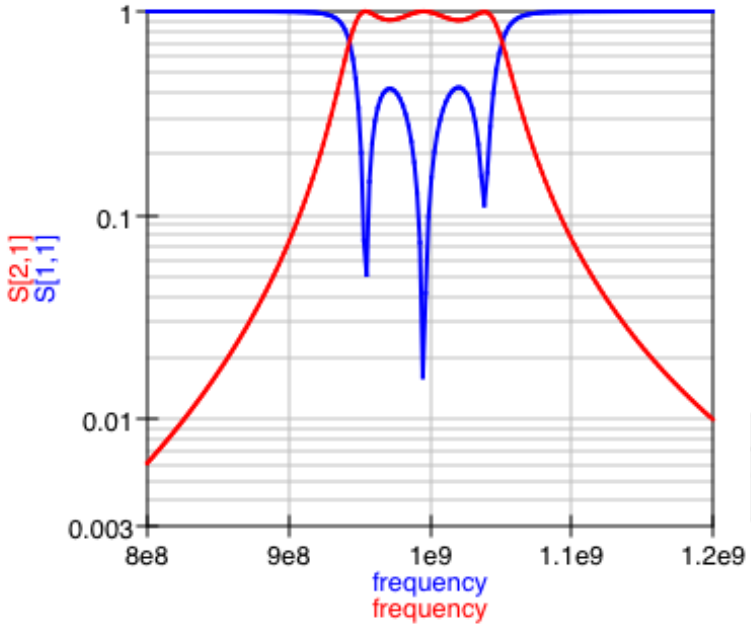


Optimization (ASCO)



S parameter simulation

SP1
Type=log
Start=800 MHz
Stop=1200 MHz
Points=200



Optimization

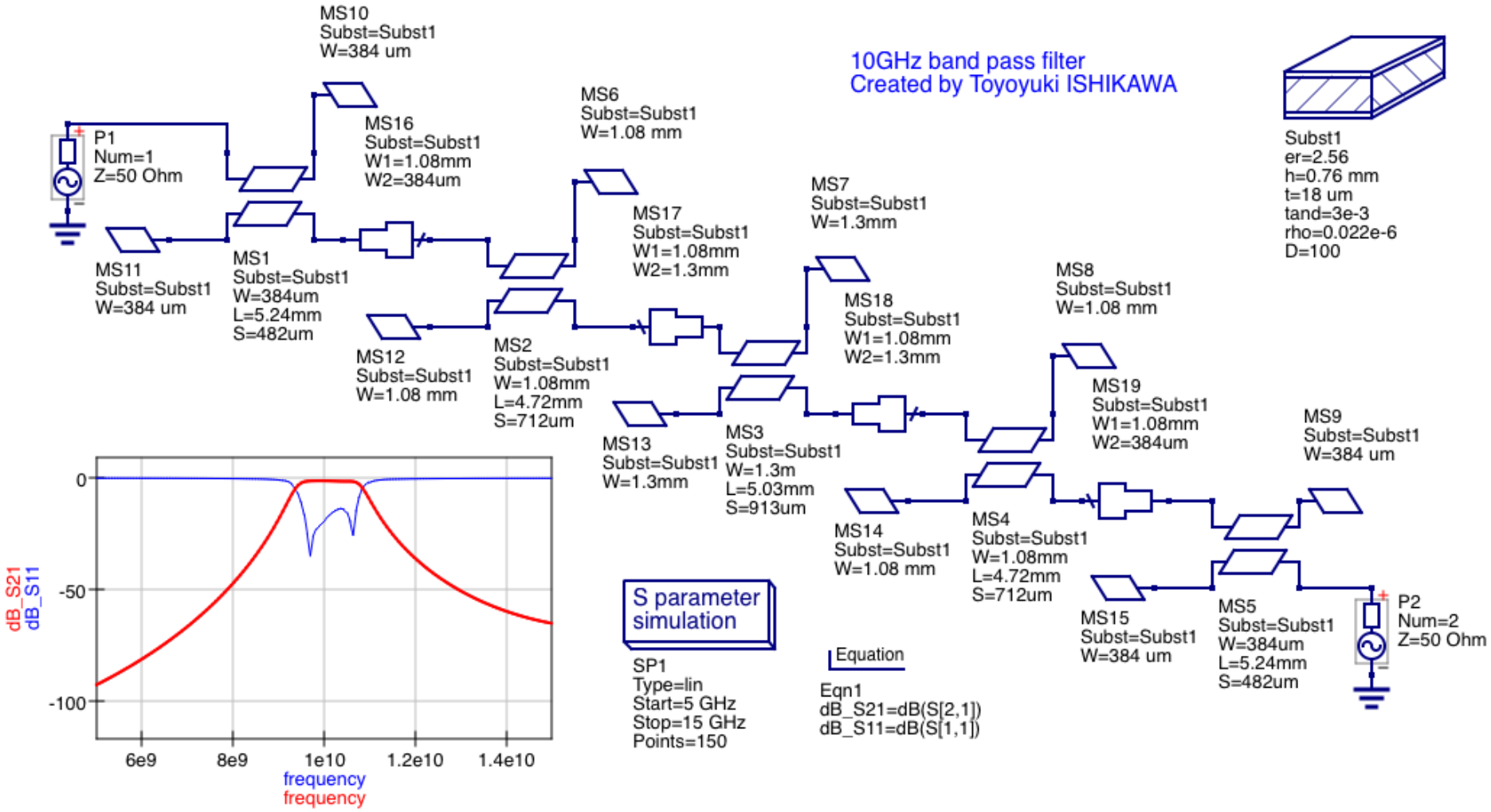
Opt1

Equation

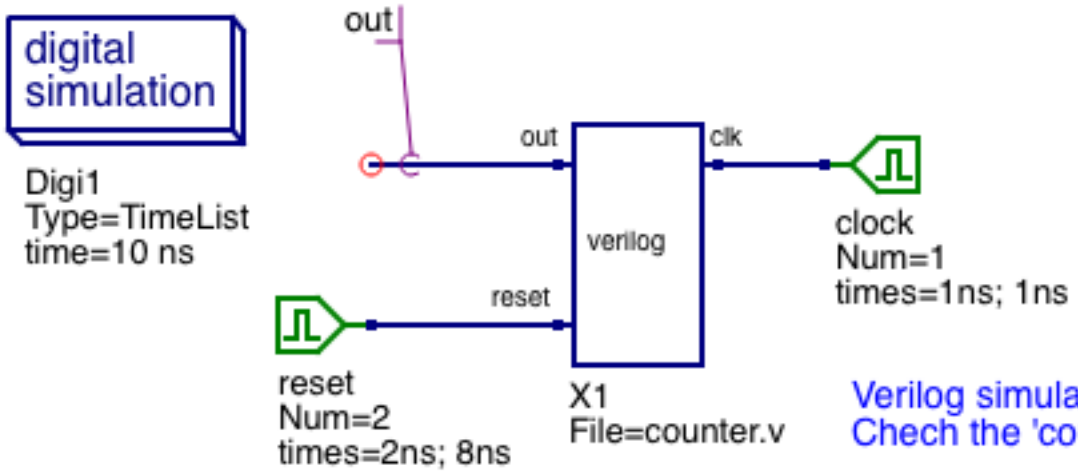
Eqn1
Left_Side_Lobe=max(dB(S[2,1]),800e6:900e6)
Pass_Band_Ripple=min(dB(S[2,1]),960e6:1040e6)
Right_Side_Lobe=max(dB(S[2,1]),1100e6:1200e6)
S11_In_Band=-max(dB(S[1,1]),960e6:1040e6)

number	Left_Side_Lobe	Pass_Band_Ripple	Right_Side_Lobe	S11_In_Band
1	-23.1	-0.856	-22.7	7.47

Microstrip band-pass filter

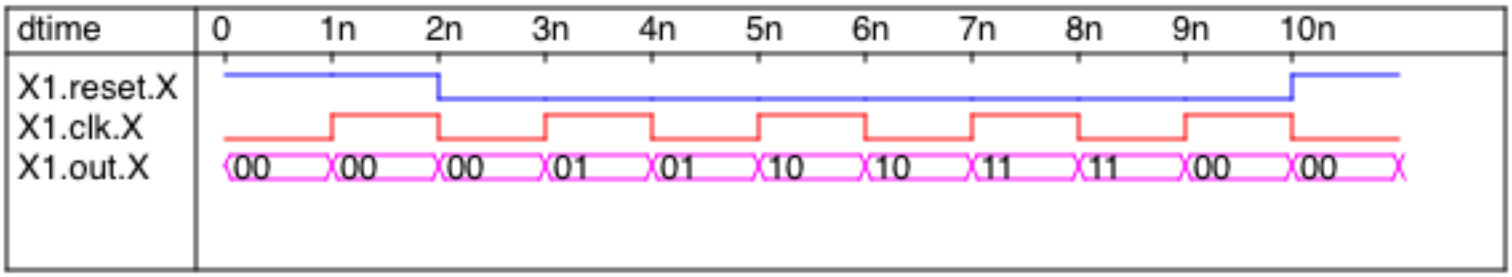


Verilog Counter




```
module counter(out, clk, reset);

  parameter WIDTH = 2;

  output [WIDTH-1 : 0] out;
  input                clk, reset;

  reg [WIDTH-1 : 0]    out;
  wire         clk, reset;

  always @(posedge clk)
    out <= out + 1;

  always @reset
    if (reset)
      assign out = 0;
    else
      deassign out;

endmodule // counter
```

Verilog simulation with Icarus Verilog
Chech the 'counter.v' for the HDL model.



Verilog-A

- Includes ~~53~~ 38 models written in Verilog-A
- Compact models
  - ~~BSIM 3, 4, 6 (Berkeley)~~
  - EKV (EPFL)
  - ~~HICUM L0, L2 (TU-Dresden)~~
  - ~~FBH-HBT (TU-Berlin)~~

CMC license issues

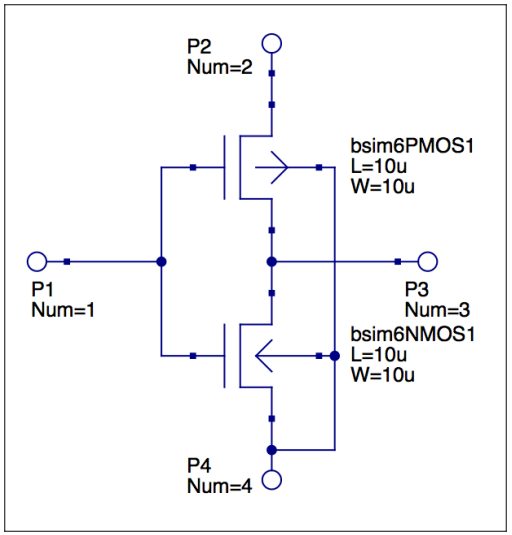
- ADMS (Automatic Device Model Synthesizer)
  - Verilog-A → XML transformations → "XYZ code"

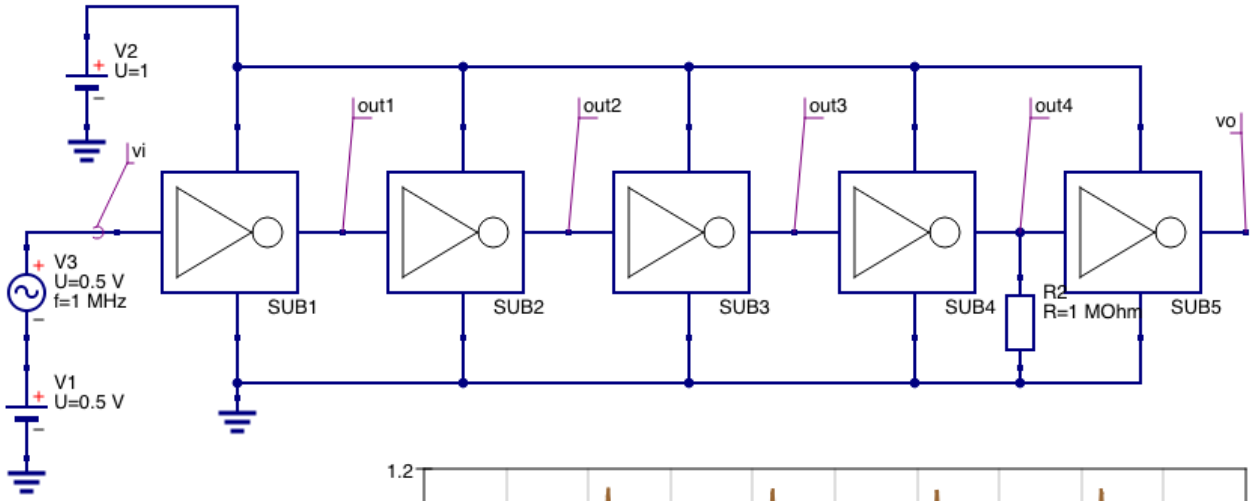
Accellera license issue

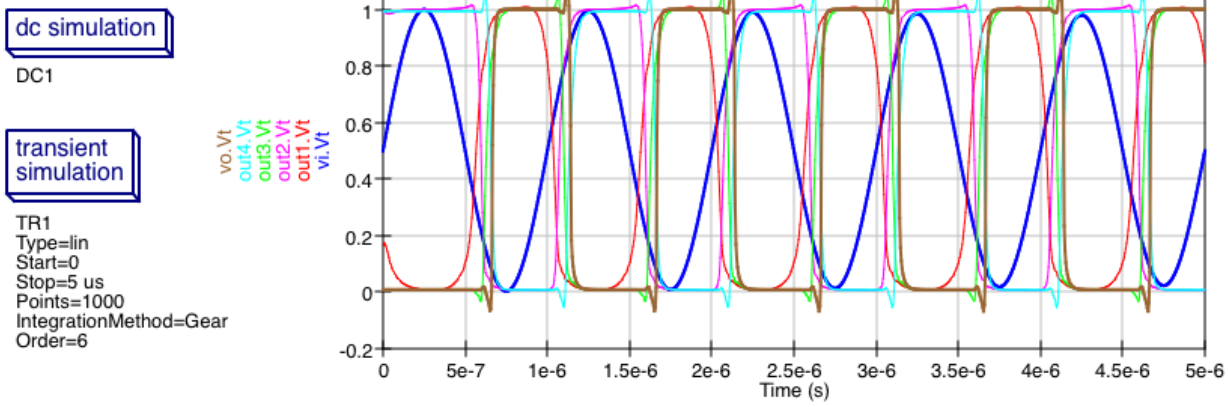
- Limitations
  - Subset of Verilog-AMS
  - Not supported: `V(n)<+ … ;`

Verilog-A model builder

- BSIM6: Qucsator x HSPICE

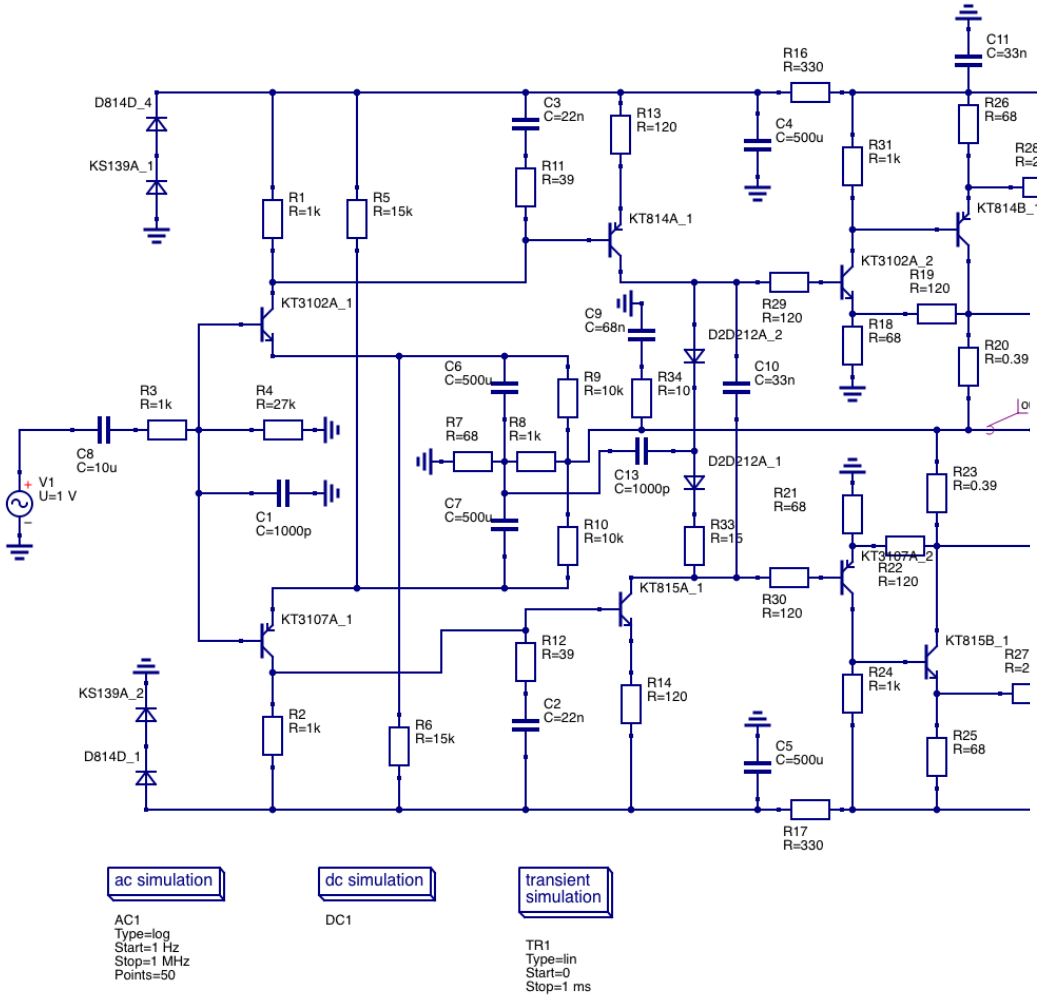


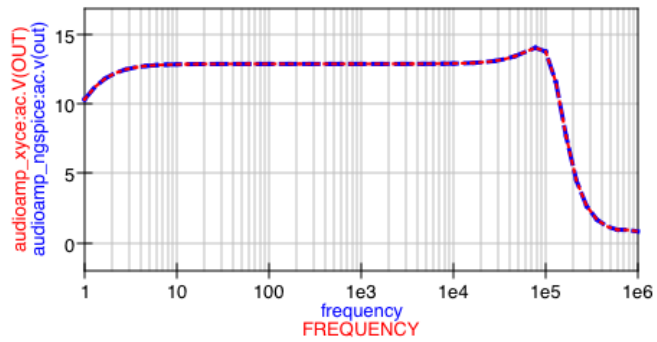


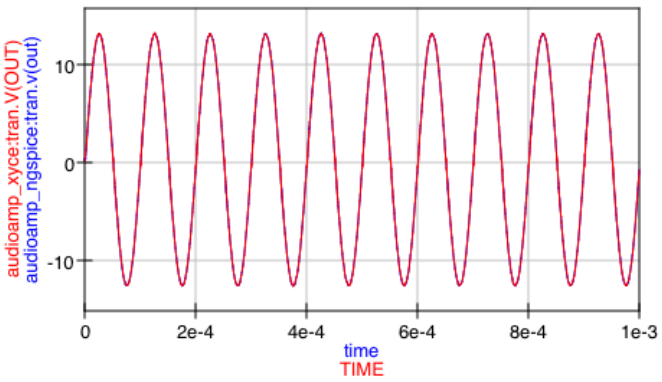


spice4qucs: Ngspice / Xyce

- Audio amplifier, troubles with Qucsator







Status

- Release 0.0.19 (February 05, 2016)
  - Bug fixing, usability improvements, build system cleanup
  - Ongoing port Qt3Support to Qt4
  - New active-filter synthesis tool
  - Integration of regression tests, qucs-test repository
  - Removal of non-GPL models
  - …
- Release 0.0.20 (no due date)
  - ~~BSIM 6~~
  - New RF models
  - spice4qucs: Ngspice (XSPICE) and Xyce frontend
    - https://github.com/Qucs/qucs/issues/77
    - https://github.com/ra3xdh/qucs/releases/tag/0.0.19S-rc3
  - Tuner, Gnucap/Gnucsator, make ADMS optional, submit package to Debian, multiple simulators…

Roadmap (whish list)

1. Simple GUI and simulator
   - Refactor/rewrite, (Qt4) Qt5, plug-ins, API…
   - Standard file formats, exchangeable
2. Powerful circuit analysis tools
   - Robust algorithms (Eigen, KLU)
   - API, high level interface (SWIG)
   - Harmonic-Balance
   - Large signal S-parameter simulation (LSSP)
   - EM field simulation / extraction (openEMS, NEC2++)
   - *SPICE flavors compatibility/converter
   - Co-simulation (analog + Verilog/VHDL), interface (icarus, GHDL)
   - Monte-Carlo simulation
   - Solvers: Ngspice, Xyce, Gnucap, SpiceOpus
3. Design and synthesis tools
   - Data import / export
4. Industry standard device models
   - MEXTRAM, VBIC, HiSIM, IGBJT, UTSOI, …
5. Hardware implementation
   - Layout PCB, device (KiCad, Klayout)

Resources

- Website: http://qucs.sourceforge.net/
- GitHub (preferred): https://github.com/Qucs/qucs/
- SourceForge: http://sourceforge.net/p/qucs/git/
- Mailing lists: http://sourceforge.net/p/qucs/mailman/
- IRC channel: #qucs
- Forum: http://sourceforge.net/p/qucs/discussion/
- Bug trackers:
  - https://github.com/Qucs/qucs/issues
  - http://sourceforge.net/p/qucs/_list/tickets
- Source code documentation:
  - http://qucs.github.io/qucs-doxygen/qucs/index.html
  - http://qucs.github.io/qucs-doxygen/qucs-core/index.html
- Downloads: http://sourceforge.net/projects/qucs/files/
- (NEW) Qucs-Help: http://qucs-help.readthedocs.org/
- (NEW) Transifex translations:
  - https://www.transifex.com/projects/p/qucs-desktop/
  - https://www.transifex.com/projects/p/qucs-help/

Final remarks

- Flexible and easy to use
- Advanced components and features
- Build and test infrastructure
- Right time for refactoring/redesign
- We are open for collaboration
- Roadmap: Your help is welcome!