Single instr. testcases → RISC-V based core model (eg Rocket)

RISC-V based core model (eg Rocket) → Per inst VCD files* → Macro-level switching information → Stressmark instruction sequence → Generate stressmarks

Generated stressmarks → RISC-V based core model (eg Rocket) → Per inst VCD files* → Macro-level switching information → Initial list of vulnerable latches → Targeted fault injection

Final list of vulnerable latches

Legend

RISC-V core RTL simulator

SERMiner

Microprobe (RISCV)

Chiffre – Latch level fault injection

*VCD – Value change dump files representing time-ordered value changes of all signals during the RTL simulation