



**Hewlett Packard**  
Enterprise

# EDK2 UEFI on RISC-V

Open Source Firmware, BMC and Bootloader Devroom

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# Agenda

- About Us
- Introduction (EDK2, RISC-V)
- History of Booting on RISC-V
- Timeline of This Implementation
- Details of Bootflow
- Demo Booting to Linux
- Status, Goals, Vision
- How to Help

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# About us

- UEFI Firmware Engineers for ProLiant Servers at HPE
- Learned a lot through this project:  
Changes required in entire UEFI/EDK2 boot flow



Abner Chang



Daniel Schaefer

- Senior UEFI Engineer
- Lead the project
- Graduated last year
- First real UEFI project

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# Disclaimer

- Work was done on company time
- But we can't speak of the strategic direction of HPE

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# UEFI and EDK2



- UEFI is only an interface specification
- EDK2 is the reference implementation of UEFI
- Initially developed for Itanium
- Now mainstream for x86\_64
- Starting to get adopted on ARM

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# RISC-V



- "Free and Open RISC Instruction Set Architecture"
- Tries to be simple and legacy-free
- Three privilege modes (**M**achine, **S**upervisor, **U**ser)
- Similar to x86, boot starts without MMU in Machine mode
- FW can stay resident after boot and be called by higher layers  
Like x86's SMM but with well defined interface like Itanium's SAL  
→ Supervisor Binary Interface (SBI)

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# History of booting on RISC-V

- 2015 BBL
- 2016 EDK2 Prototype with QEMU RISC-V PC/AT board<sup>[5]</sup>
- 2017 U-Boot
- 2018 U-Boot with UEFI interface
- 2018 Coreboot
- 2019 Oreboot
- 2020 EDK2+OpenSBI Upstream

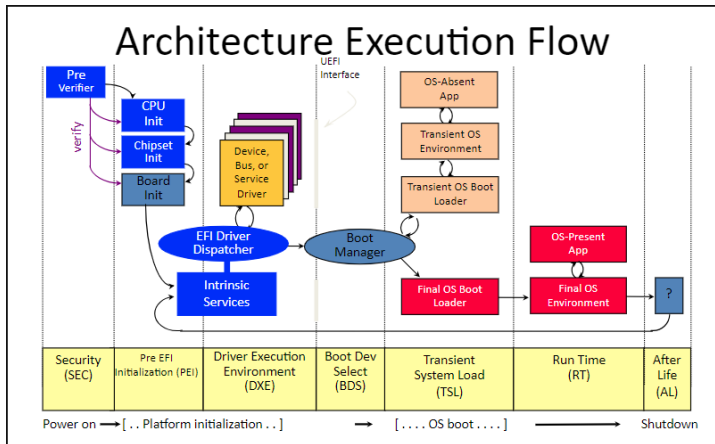
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# Timeline of this implementation

- 2015 Started at HPE
- 2016 Prototype presented at UEFI Forum Plugfest
- 2020 Initial upstreaming to EDK2  
Booting to UEFI shell on Hifive Unleashed
- 2021 Upstream Linux EFISTUB support (WIP)
- 2021 Port more boards, e.g. BeagleV (WIP)



# UEFI Phases



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# Reset at ZSBL

## Walkthrough of Hifive Unleashed Bootflow

- Starts running in M-Mode without MMU
- ZSBL (zero stage bootloader)
- Embedded in mask ROM or hardcoded in QEMU source
- Jumps to predefined address

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## SEC - First Phase of UEFI (ASM)

- Fully custom for RISC-V
  - Starts in assembly
1. Set up scratch register (mscratch)
  2. Set up stack in temporary RAM
  3. Set up trap handler to preserve registers and call OpenSBI
  4. Calls SEC core C function with hartid and scratch pointer

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## SEC - First Phase of UEFI (C)

1. Add UEFI private region in scratch space
  - Machine information (march, mimpid, ...)
2. Initialize OpenSBI (sbi\_init)
  - Stall non-booting harts

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# SEC - Initialize OpenSBI

1. Pass scratch pointer with
  - Device Tree
  - Next mode (M-Mode still)
  - Platform specific functions
2. Register custom SBI calls (avoid linking PEI to OpenSBI)

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# SEC - Switch to PEI

1. Find PEI entrypoint in firmware volume
2. Switch to S-Mode
3. Enable identity mapped MMU
4. Jump to PEI and pass it information about
  - Boot firmware volume
  - Temporary ram
  - Stack

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# PEI

From here on most of the code is arch-agnostic in EDK2.

1. Discover RAM and migrate there
2. Dispatch PEIMs
  - Take device tree from scratch space and store in HOB
  - Discover processor features and store in HOB (For SMBIOS)
  - Others ...
3. Build new stack
4. Switch stack and execute DxeIpl

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## DXE - Dispatch DXEs

- Install timer interrupt handler and DXE Protocol
- Install RuntimeServices (WIP)
- Install SMBIOS tables using information from PEI
  - Type 4 (CPU)
  - Type 7 (Caches)
  - **Type 44** (Additional CPU information)
- Install device tree
  - Extract from HOB
  - Insert boot hartid (required by Linux)
  - Insert into EFI System Configuration Table



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# BDS - UEFI Shell

Not upstream yet.

Prep: Embed EFISTUB and initrd disk image in flash image

1. Load disk into memory and turn into ramdisk with shell command
2. Install initrd on handle of fixed device path ('initrd')
3. Execute EFISTUB

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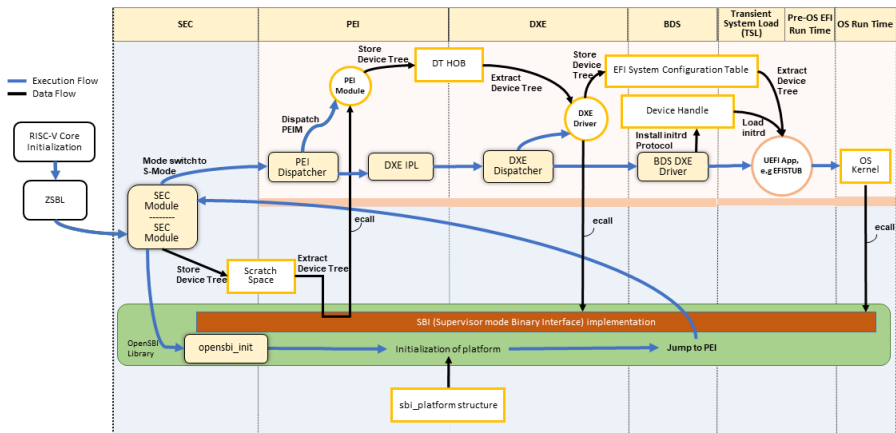
# EFISTUB - Since Linux 5.10

Implemented by Atish Patra, tested and finalized in cooperation with us

1. Take device tree from EFI System Configuration Table
2. Call LoadFile2 on device path to extract initrd
3. Execute kernel proper
  - Disable MMU
  - `jump_kernel(hartid, fdt);`


# RISC-V EDK2 Phases

## EFI Execution Phases



# Demo Booting to Linux

```
$ cat runqemu.sh
#!/bin/sh
qemu-system-riscv64 -machine sifive_u \
  -bios ./Build/FreedomU540HiFiveUnleashed/DEBUG_GCC5/FV/U540.fd \
  -m 2048 -nographic -smp cpus=4,maxcpus=4
$
```



<https://asciinema.org/a/KPDSvhXNVTbsQ45oRUVEu81nY>

Firmware image at <https://github.com/riscv/riscv-uefi-edk2-docs/releases>

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# Status - EDK2

- UEFI Shell
- UEFI Applications (e.g. bootloader)
- Booting Linux via EFISTUB

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## Status - Platforms

Platform Name	UEFI Shell	Linux
HiFive Unleashed	Yes	Yes
QEMU sifive_u	Yes	Yes
Freedom U500 FPGA	Yes	N/A
QEMU virt	N/A	N/A
Andes AE350	N/A	N/A
BeagleV	N/A	N/A

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## Status - Overall

- UEFI specification amended
- SMBIOS specification amended
- EDK2 port merged upstream
- Linux EFISTUB ported by Atish, merged in 5.10
- UEFI Self Certification Test ported, patches need cleanup

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# Goals

- Implement *ResetSystem* Runtime Service with SBI (WIP)<sup>[1]</sup>
- Upstream changes for booting Linux (FDT fixup and storing)
- SD card driver for Hifive Unleashed
- Implement new relocation types by newer GNU toolchains<sup>[2]</sup>
- Build "OVMF" for QEMU's virt platform with VirtIO drivers<sup>[3]</sup>
  - Add boot tests to EDK2 CI
  - Boot with actual disk!
- Port to BeagleV when it arrives<sup>[4]</sup>
- SecureBoot?



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# How to Help

- Port to more boards, talk to us
- Check out the issues on the repo
- Spread the word

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# Vision for the Future

- Make RISC-V boot like rest of industry  
U-boot for embedded, UEFI for consumer and server
- Follow in ARM's footsteps to *make booting boring*
- Encourage discussion about desktops and servers

# Thanks

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**Thanks for listening!**

Check us out on GitHub:

Development

Upstream

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riscv/riscv-uefi-edk2-docs

riscv/riscv-edk2

riscv/edk2-platforms

tianocore/edk2

tianocore/edk2-platforms

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# References

UEFI and PI Spec  
SBI Spec

<https://www.uefi.org/specifications>

<https://github.com/riscv/riscv-sbi-doc>

- [1] SBI SystemReset
- [2] GOT relocation
- [3] RISC-V OVMF
- [4] BeagleV
- [5] EDK2 RISC-V in 2016

<https://github.com/riscv/riscv-sbi-doc/commit/2f101582210b17a6>

<https://github.com/riscv/riscv-edk2/issues/3>

<https://github.com/riscv/riscv-edk2/issues/2>

<https://beagleboard.org/beaglev>

<https://www.youtube.com/watch?v=9c73WHduovs>

BBL  
OpenSBI  
U-Boot  
Coreboot  
Oreboot  
QEMU  
Itanium SAL/PAL

<https://www.lowrisc.org/docs/build-berkeley-boot-loader/>

<https://github.com/riscv/opensbi>

<https://www.denx.de/wiki/U-Boot>

<https://coreboot.org/>

<https://github.com/oreboot/oreboot>

<https://www.qemu.org/>

<https://www.csee.umbc.edu/portal/help/architecture/24535901.pdf>

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# Glossary

UEFI	Unified Extensible Firmware Interface
EDK2	UEFI's reference implementation
Tianocore	Umbrella name of EDK2 and related projects
MMU	Memory Management Unit
SBI	RISC-V interface between S and M-mode
Itanium	First 64 bit processor by Intel
SAL	Itanium's System Abstraction Layer
RISC	Reduced Instruction Set Computer (vs CISC)
SMM	System Management Mode
HPE	Hewlett Packard Enterprise