Real-time Netlisting in KiCad

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Crash Course in Schematic Jargon

Pins

Net Wire

Component
Crash Course in Schematic Jargon

**Net:**
A set of connected pins with a name
Backstory: Bus Upgrades
Bus Unfolding

How do we know what to put in this menu?
But the Highlight tool already exists...?
This doesn’t scale well...
Real-time Netlisting in KiCad
Connectivity Algorithm at a High Level

1. What is graphically connected?

   ![Graphically connected nodes TP1 and TP2](image1)

2. What is connected by labels?

   ![Nodes connected by labels TP1, A0, and TP2](image2)

3. What about the hierarchy?

   ![Hierarchy with Subsheet, ADDR, A0, and TP3](image3)
What is Graphically Connected?
What is Connected by Labels?

Driver
# Hierarchy of Drivers

<table>
<thead>
<tr>
<th>Driver Type</th>
<th>Label Scope</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Pin</td>
<td>Global</td>
<td>Net-(R1-Pad1)</td>
</tr>
<tr>
<td>Hierarchical Sheet Pin</td>
<td>Local</td>
<td>/sheet/path/A</td>
</tr>
<tr>
<td>Hierarchical Label</td>
<td>Local</td>
<td>/sheet/path/B</td>
</tr>
<tr>
<td>Local Label</td>
<td>Local</td>
<td>/sheet/path/C</td>
</tr>
<tr>
<td>Power Symbol Pin</td>
<td>Global</td>
<td>GND</td>
</tr>
<tr>
<td>Global Label</td>
<td>Global</td>
<td>MY_NET</td>
</tr>
</tbody>
</table>
What is Connected by Labels?

Power Symbol (fancy label)
Handling Hierarchical Designs

File: cpu.kicad_sch

Label D0
Orientation Horizontal left
Style Normal
Size 0.050 in
Connection Name /DATA0
Managing Complexity

1. Bug Report
2. Code Change
4. Regression
<table>
<thead>
<tr>
<th>Design</th>
<th>KiCad 5.1</th>
<th>KiCad 5.99</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design A</td>
<td>240 ms</td>
<td>57 ms</td>
<td>-76%</td>
</tr>
<tr>
<td>35 sheets</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design B</td>
<td>180 ms</td>
<td>81 ms</td>
<td>-50%</td>
</tr>
<tr>
<td>13 sheets</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design C</td>
<td>625 ms</td>
<td>150 ms</td>
<td>-76%</td>
</tr>
<tr>
<td>10 sheets</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Unanticipated Benefits

<table>
<thead>
<tr>
<th>Line Type</th>
<th>Line Style</th>
<th>Connection Name</th>
<th>Assigned Netclass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire</td>
<td>solid</td>
<td>/SDA0</td>
<td>Default</td>
</tr>
<tr>
<td>Z 12.01</td>
<td>X 4.200 Y 4.300</td>
<td>dx 4</td>
<td></td>
</tr>
</tbody>
</table>
Improving Electrical Rule Checks

Electrical Rules Checker

- Label not connected to anything
  - Label ‘GRANDCHILD_A0’
  - Label ‘GRANDCHILD_A2’

- Both GCIB0 and GCOB2 are attached to the same items; GCIB0 will be used in the netlist
  - Label ‘GCIB0’
  - Label ‘GCOB2’

- Label not connected to anything
  - Label ‘GRANDCHILD_IN_C1’
  - Label ‘GRANDCHILD_OUT_C1’

Show: □ All  □ Errors 19 □ Warnings 9 □ Exclusions

Delete Markers  Close  Run ERC
Opportunities for Improvement

Make it even faster!

- Incremental updates
- Caching hierarchical sheet information
- Refactoring for performance
Real-time ERC

More than one label on this net!