

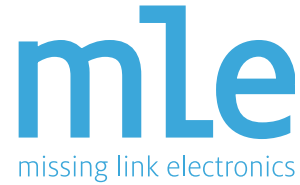


CORUNDUM

An open source FPGA based 100G NIC



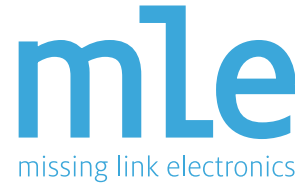
Overview



- 1) Introduction
- 2) RTL/ Drivers
- 3) Outlook / Roadmap



About Us



Alex

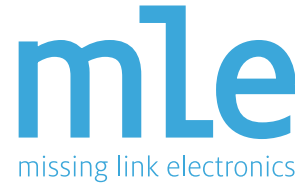
- Ph.D. EE UC San Diego
- M.Sc. & B.Sc. EE UC San Diego
- Post Doctoral Researcher at UC San Diego
- Main developer of corundum
- Aims at supporting research driven features

Ulrich

- Dipl.-Ing. Computer Engineering TU Berlin
- Dir. Eng. at Missing Link Electronics
- Team lead of a design team integrating and extending corundum
- Aims at providing a reliable source for a data center ready NIC



Background



- Academic project to enable network architecture research experiments at full speed
- Work was part of the Dissertation Thesis of Dr. John Alexander Forencich (Alex) at UC San Diego and released to open source
- Presented at various academic conferences, including FCCM 2020



Goals

- Line-rate capable NIC
- Portable RTL and Linux Driver code
- Support for various variants of interconnects, e.g. PCIe and AXI-MM
- Fully open source
- Adaptable for academic and commercial projects

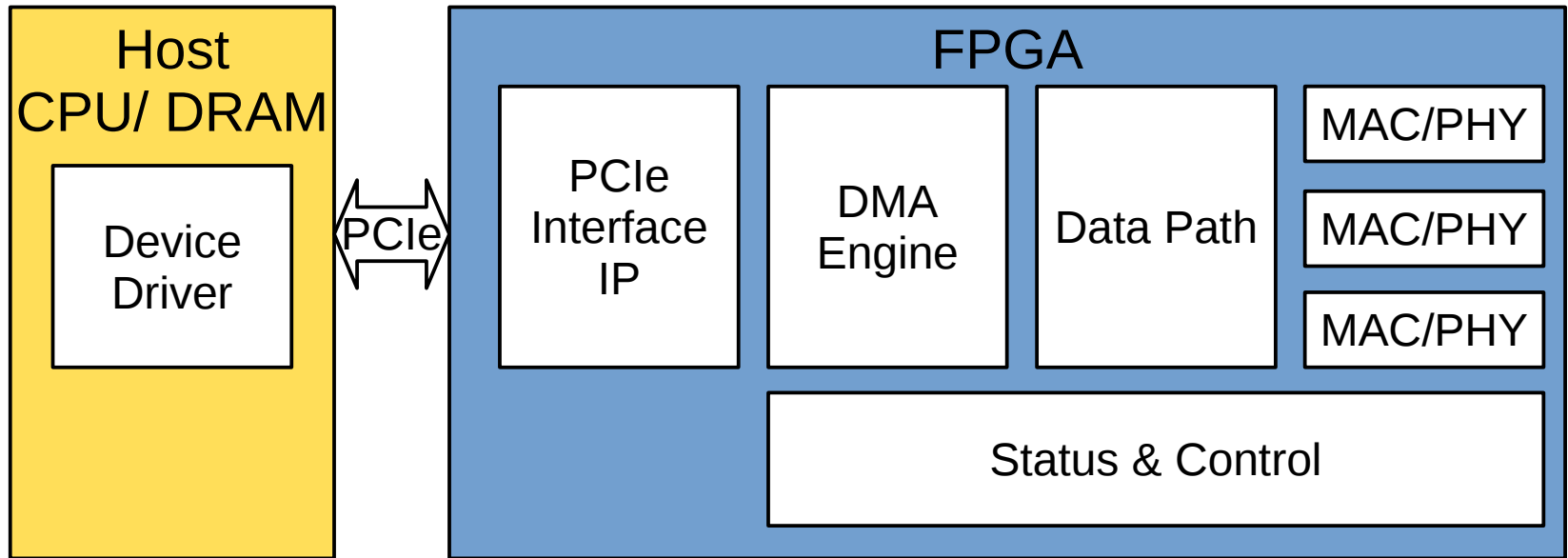


Features

- PCIe attached NIC
- 1-8x (1/)10/25/100 GbE physical Ports
- Driver for Linux
- > 16k rings supported for RX and TX
- Custom scheduling, processing logic addition in RTL and driver
- Full Xilinx UltraScale+ device support
- Initial Intel Stratix 10 (H-Tile) device support
- Various Supported Boards
 - Xilinx: ADM_PCIE_9V3, AU250, AU50, ExaNIC_X25, NetFPGA_SUME, VCU108, VCU1525, AU200, AU280, ExaNIC_X10, fb2CG, VCU118, ZCU106
 - Intel: S10MX_DK



Overview





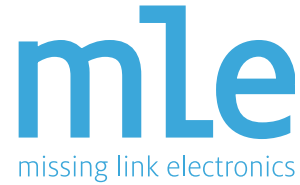
Background

Corundum is based on various (sub-) projects and components (partially also maintained by Alex)

- [verilog-axi](#)
- [verilog-axis](#)
- [verilog-pcie](#)
- [verilog-ethernet](#)
- [cocotb](#)
- [MyHDL](#)
- Device Specific Vendor IP



Overview



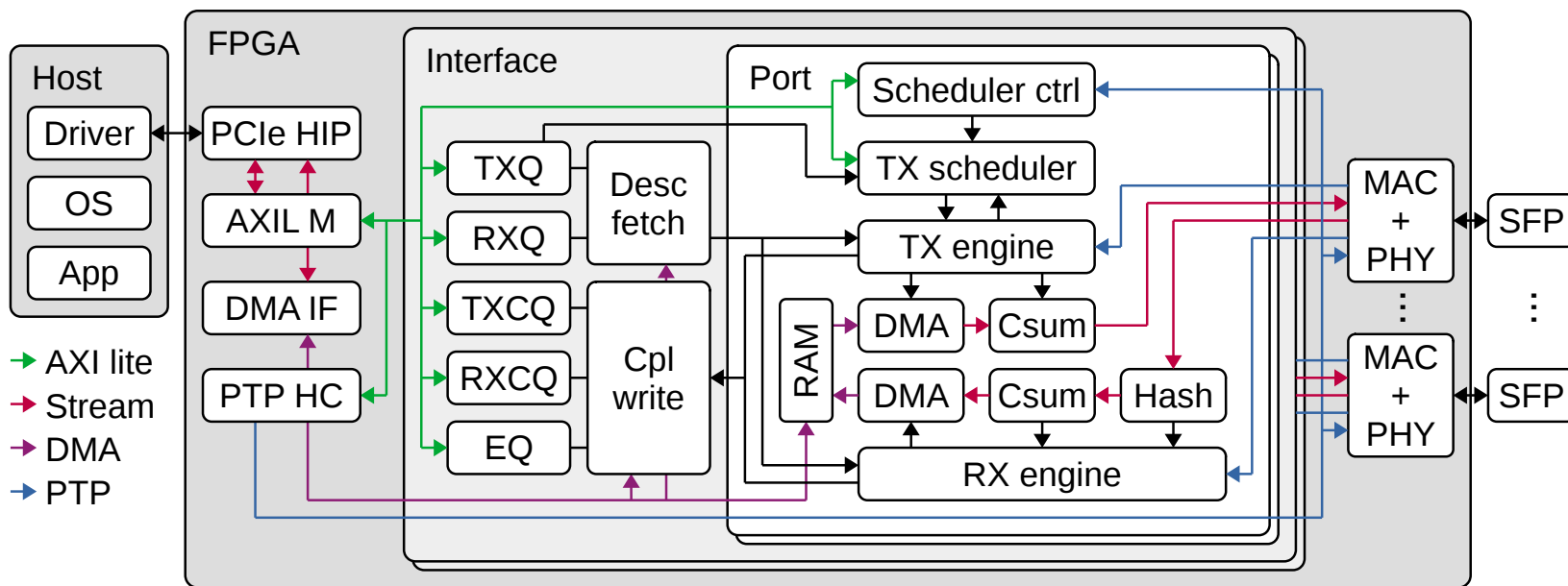
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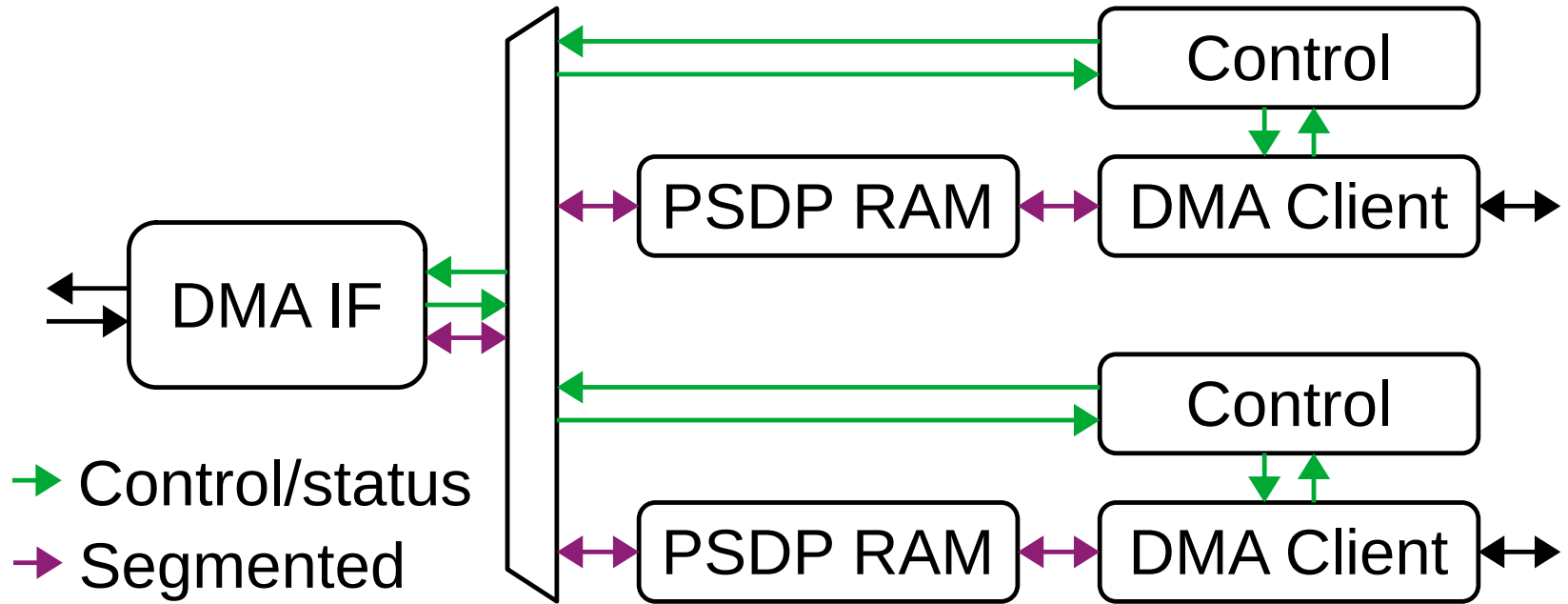


RTL Structure





DMA RTL Structure





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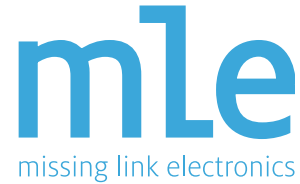


Roadmap

- Restructure RTL (shared datapath)
- SW/HW Interface Optimisation (Variable Length Descriptors)
- Unified DMA Address Space (Host + on-board DRAM)
- RDMA Support
 - RoCEv2
 - On-board DRAM Cache
- DPDK Support
- Large Send Offload (LSO)/ Large Receive Offload (LRO)



Meet Us



- Mailing list:
<https://groups.google.com/d/forum/corundum-nic>
- Slack:
https://join.slack.com/t/corundumworkspace/shared_invite/zt-tj5azsbm-V9LV8L7ugSRDBpe2JiPKMA
- Developer Meeting bi-weekly (Mon 6 pm MEZ):
<https://github.com/corundum/corundum/wiki/Corundum-Developer-Meeting>
- Github Repo:
<https://github.com/corundum/corundum>
- Github WIKI:
<https://github.com/corundum/corundum/wiki>