ROCgdb, GDB and AMDGPU debugging

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Agenda

• AMDGPU architecture overview and programming model.
• ROCgdb.
• State of AMDGPU support in upstream GDB.
Abstract AMDGPU architecture

- Multiple processing elements form a compute unit.
- Multiple compute units form a GPU.
# The HIP "hello world"

```cpp
#include <hip/hip_runtime.h>

__global__ void kern (int *arr) {
    arr[blockIdx.x * blockDim.x + threadIdx.x] += 2;
}

int main () {
    const size_t block_size = 64, blocks = 16,
                     size = block_size * blocks;
    std::array<int, size> data = {};

    int *device_ptr;
    hipMalloc (&device_ptr, size * sizeof(int));
    hipMemcpyHtoD (device_ptr, data.data (), size * sizeof(int));

    kern<<<blocks, block_size>>> (device_ptr);

    hipMemcpyDtoH (data.data (), device_ptr, size * sizeof(int));
    return EXIT_SUCCESS;
}
```
Host threads and GPU threads (waves) under single inferior

- Waves are mapped to threads in GDB.
- Same program with unified memory.

(gdb) info threads

<table>
<thead>
<tr>
<th>Id</th>
<th>Target Id</th>
<th>Frame</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Thread 0x7ffff7e69a80 (LWP 152926) &quot;a.out&quot;</td>
<td>0x...f41 in ?? () from .../libhsa-runtime64.so.1</td>
</tr>
<tr>
<td>2</td>
<td>Thread 0x7ffffbeb3ff640 (LWP 152929) &quot;a.out&quot;</td>
<td>__GI___ioctl (fd=3, request=3222817548) ...</td>
</tr>
<tr>
<td>5</td>
<td>Thread 0x7fffff62d7640 (LWP 152933) &quot;a.out&quot;</td>
<td>__GI___ioctl (fd=3, request=3222817548) ...</td>
</tr>
<tr>
<td>*6</td>
<td>AMDGPU Wave 1:1:1:1 (0,0,0)/0 &quot;a.out&quot;</td>
<td>kern (arr=0x7fffffff00000) at simple.cpp:5</td>
</tr>
<tr>
<td>7</td>
<td>AMDGPU Wave 1:1:1:2 (0,0,0)/1 &quot;a.out&quot;</td>
<td>kern (arr=0x7fffffff00000) at simple.cpp:5</td>
</tr>
<tr>
<td>8</td>
<td>AMDGPU Wave 1:1:1:3 (1,0,0)/0 &quot;a.out&quot;</td>
<td>kern (arr=0x7fffffff00000) at simple.cpp:5</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>
GPU Threads (waves)'s Target Id

(gdb) info threads
...
     agent
   queue
 dispatch
|  wave id
|   |  
6  AMDGPU Wave 1:1:1:1 (0,0,0)/0 "a.out" kern (arr=0x7fffe9c00000) at simple.cpp:5
    ^^^^^  |
     |  \- wave number in work group
     \- work group coordinates in work grid
...

• "info {agent, queue, dispatch}" commands also available.
Lanes

New entity under threads: threads become vectorized, multiple lanes under one thread.

GDB threads are mapped to GPU waves. All lanes progress side-by-side forming a wavefront.

One physical PC for the whole thread (for all lanes), but:
- Each lane works with its own slice of the register set, on its share of data, its version of locals in scope.
- Lanes can be seen as multiple "regular" threads running in lockstep.

"current lane" concept added (augmenting "current inferior", "current thread").
Lanes commands

(gdb) info lanes

<table>
<thead>
<tr>
<th>Id</th>
<th>State</th>
<th>Target Id</th>
<th>Frame</th>
</tr>
</thead>
<tbody>
<tr>
<td>* 0</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/0 (0,0,0)[0,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>1</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/1 (0,0,0)[1,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/2 (0,0,0)[2,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>3</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/3 (0,0,0)[3,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>4</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/4 (0,0,0)[4,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>5</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/5 (0,0,0)[5,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>6</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/6 (0,0,0)[6,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
<tr>
<td>...</td>
<td>A</td>
<td>AMDGPU Lane 1:1:1:1/31 (0,0,0)[31,0,0]</td>
<td>kern (arr=0x7fffe9c00000) ...</td>
</tr>
</tbody>
</table>

(gdb) lane 8

[Switching to thread 6, lane 8 (AMDGPU Lane 1:1:1:1/8 (0,0,0)[8,0,0])]

#0 kern (arr=0x7fffe9c00000) at simple.cpp:5
5 arr[blockIdx.x * blockDim.x + threadIdx.x] += 2;
SIMT Lanes's Target Id

/ - agent
  | / - queue
  | | / - dispatch
  | | | / - wave id
  | | | |
  | | | |
  | | | |
  | | | |
  | | | |
AMDGPU Lane 1:1:1:1/8 (0,0,0) [8,0,0] kern (arr=0x7fffe9c00000) at simple.cpp:5
  | ^^^^^^  ^^^^^^
SIMT and Lane divergence

if (foo (lid)) {
    elem = in[lid] + 1;
} else {
    elem = in[lid] + 3;
}

// if (foo (lid)) {
    NoOp;
// } else {
    // } elem = in[lid] + 3;
// }
Without lane divergence support, step 1

Stepping stops in all branches => surprising

```c
__device__ void function (unsigned tid, const int *in, int *out)
{
    int elem;

    if (tid % 2) // (1)
        elem = in[tid] + 1; // (3)
    else // (2)
        elem = in[tid] + 3;

    atomicAdd (out, elem); // (4)
}
```
Without lane divergence support, step 2

Stepping stops in all branches => surprising

```c
__device__ void function (unsigned tid, const int *in, int *out)
{
    int elem;

    (1)   if (tid % 2)
    (3)    elem = in[tid] + 1;
    else
    >> (2)    elem = in[tid] + 3;  <<<<<<<<<<<
    (4)   atomicAdd (out, elem);
}
```
Without lane divergence support, step 3

Stepping stops in all branches => surprising

```c
__device__ void function (unsigned tid, const int *in, int *out) {
    int elem;

    (1) if (tid % 2)
    >> (3)   elem = in[tid] + 1;  
    <<< (2)   elem = in[tid] + 3;
    (4) atomicAdd (out, elem);
}
```
Without lane divergence support, step 4

Stepping stops in all branches => surprising

```cpp
__device__ void
function (unsigned tid, const int *in, int *out)
{
    int elem;

    (1) if (tid % 2)
    (3)   elem = in[tid] + 1;

    else
    (2)   elem = in[tid] + 3;

    >> (4) atomicAdd (out, elem);  <<<<<<<<<
}
```
With lane divergence support, step 1

Stepping doesn't stop if current lane is inactive => intuitive

```c
__device__ void
function (unsigned tid, const int *in, int *out)
{
    int elem;

    >> (1) if (tid % 2) <<<<<<<<<<<
    (X)   elem = in[tid] + 1;
    else
        (2)   elem = in[tid] + 3;
    (3)   atomicAdd (out, elem);
}
```
With lane divergence support, step 2

Stepping doesn't stop if current lane is inactive => intuitive

```c
__device__ void
function (unsigned tid, const int *in, int *out)
{
    int elem;

    (1)  if (tid % 2)
(X)        elem = in[tid] + 1;
    else

(2)  >> elem = in[tid] + 3;

(3)  <<< atomicAdd (out, elem);
}
```
With lane divergence support, step 3

Stepping doesn't stop if current lane is inactive => intuitive

```c
__device__ void
function (unsigned tid, const int *in, int *out)
{
    int elem;

    (1) if (tid % 2)
    (X)    elem = in[tid] + 1;
    else
    (2)    elem = in[tid] + 3;
    >> (3) atomicAdd (out, elem);   <<<<<<<<<
}
```
Multiple address spaces support

- Introducing the address_space+offset notation.
- Architecture address-spaces are not a source language concept!
- Use "maintenance print address-spaces " to list the address-spaces supported by the current target.

```c
__device__ int some_global = 8;
__shared__ int some_shared;

__device__ int
func (int *arr)
{
    int some_private = 8;
    return some_shared + some_private;
}
```

```c
(gdb) p &some_global
$1 = (int *) 0x7fffffff617d1a8 <some_global>
(gdb) p &some_shared
$2 = (int *) local#0x0
(gdb) p &some_private
$3 = (int *) private_lane#0x40
(gdb) x private_lane#0x40
private_lane#0x40: 0x00000008
(gdb) p *(int*)private_lane#0x40
$4 = 8
```
Useful things to know

• Exceptions are reported for the entire wave.

• Memory exceptions are not precise by default.
  • If available, use "set amdgpu precise-memory on" to identify the faulty instruction (impacts performances).

• On some architectures, attaching to a process shows:
  
  `AMDGPU Wave 1:3:?:1 (?,?,?)/? "attached_process" ...`

  • Use "HSA_ENABLE_DEBUG=1" before starting the process.

• On some architectures, at most one process can be debugged at a time.
DWARF and GPU architectures

• Challenges with current DWARF standard:
  o AMD GPUs have multiple address spaces, a "numerical address" is not sufficient to locate an object in memory.
  o The stack is not implemented in the default address space.
  o Support for divergent control flow of SIMT hardware.
  o And more…

• DWARF extensions to overcome those issues implemented in downstream LLVM + ROCgdb:
  o https://llvm.org/docs/AMDGPUDwarfExtensionsForHeterogeneousDebugging.html

• "DWARF for GPU" workgroup involving multiple vendors working to propose changes to the DWARF committee:
  o https://dwarfstd.org/issues/230524.1.html
  o More to come…
# AMDGPU support status in upstream GDB

<table>
<thead>
<tr>
<th>Feature</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver support in upstream Linux kernel</td>
<td>✓</td>
</tr>
<tr>
<td>Wave control (breakpoint, single-step, interrupt &amp; resume)</td>
<td>✓</td>
</tr>
<tr>
<td>Disassembly</td>
<td>✓</td>
</tr>
<tr>
<td>Precise memory-operations</td>
<td>✓</td>
</tr>
<tr>
<td>Displaced stepping</td>
<td>Pending</td>
</tr>
<tr>
<td>Stack unwinding</td>
<td>Blocked by DWARF</td>
</tr>
<tr>
<td>Printing variables</td>
<td>Blocked by DWARF</td>
</tr>
<tr>
<td>Address spaces support</td>
<td>Blocked by DWARF</td>
</tr>
<tr>
<td>Lane debugging</td>
<td>Need to agree with other vendors on the UI. Need DWARF to write testcases.</td>
</tr>
<tr>
<td>Watchpoints</td>
<td>Need DWARF to write testcases</td>
</tr>
</tbody>
</table>
Additional resources

- ROCgdb:
  - [https://github.com/ROCm/ROCgdb/](https://github.com/ROCm/ROCgdb/)
- Rocm-dbgapi (used by GDB to control AMDGPU devices):
  - [https://github.com/ROCm/ROCdbgapi/](https://github.com/ROCm/ROCdbgapi/)
- "Anatomy of ROCgdb" at GNU Cauldron 2022:
  - [https://www.youtube.com/watch?v=X1iZ_Ta7jOo](https://www.youtube.com/watch?v=X1iZ_Ta7jOo)
- "DWARF extensions for optimized SIMT/SIMD (GPU) debugging" at Linux Plumbers Conference 2021:
  - [https://lpc.events/event/11/contributions/1012/](https://lpc.events/event/11/contributions/1012/)
  - [https://www.youtube.com/watch?v=Iv2WO67nklc](https://www.youtube.com/watch?v=Iv2WO67nklc)
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