All Open Source Toolchain for ZYNQ 7000 SoCs

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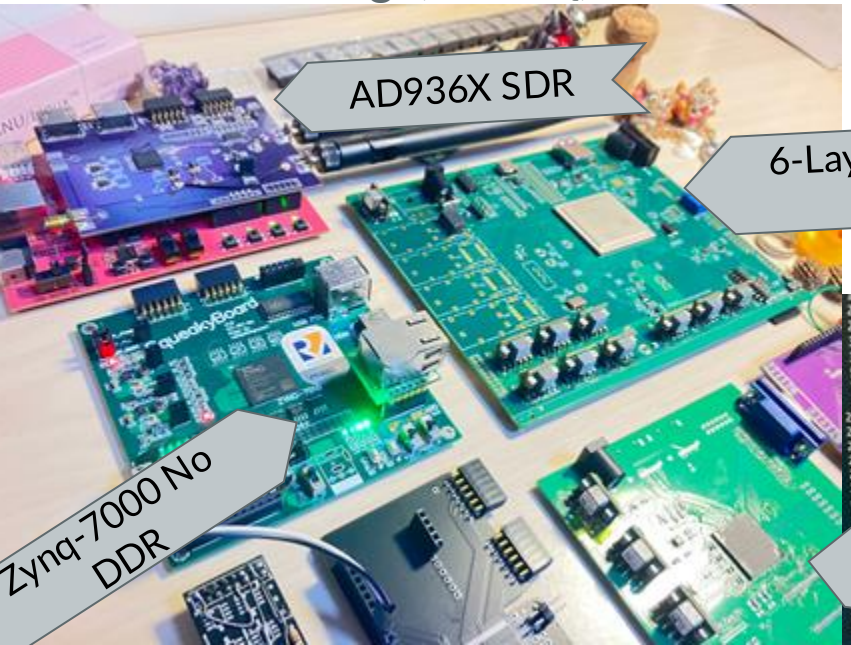
Embedded, Mobile and Automotive devroom,
FOSDEM 2025

About Me

- PhD candidate
- Amateur FPGA programming, RISC-V, PCB design, ZYNQ, Maker Faire, etc



MMU/No-MMU 32-bit RISC-V SoC

Table of Contents

Open-source FPGA Toolchains

From iCE40 to Kintex 7

- Icestorm for **Lattice iCE40**, in 2015
- PrjTrellis for **Lattice ECP5**
- Project Apicula for **Gowin**
- F4PGA for **Xilinx 7 Series**
- OpenXC7 supports **Kintex 7**

- ice40hx8k, 8K LE
- lfe5u-85f, 85K LE
- gw2ar, 20K LE
- xc7a200t, 200K LE
- xc7k480t, 480K LE

https://github.com/openXC7/

Possibilities

- PicoRV32, KianRiscV, Quasi SoC (No-MMU), UberDDR3, SD Card, HDMI, MMCM, IOSERDES
- Spartan 7/Artix 7/Kintex 7, **Zynq 7000 PL (Artix and Kintex fabric)**
- SATA controller, 10G ETH, GTP, GTX, PCIe

Runs on ARM Machines (Apple M1 included)

Runs in Docker

Runs for online services

docker pull regymm/openxc7 (openxc7-arm)
docker pull regymm/gowin
docker pull regymm/oss-cad-suite

Now Zynq!

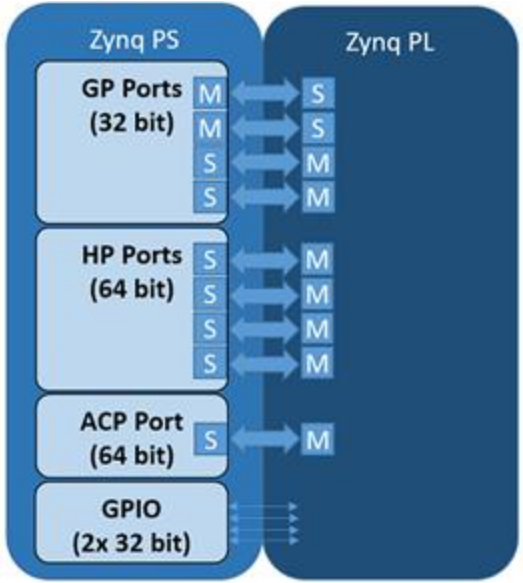
Double trouble?

- “Unique” PS + PL structure

2x ARM A9, DDR3
ETH/USB/…
Flexible pins

Linux / RTOS

Boot



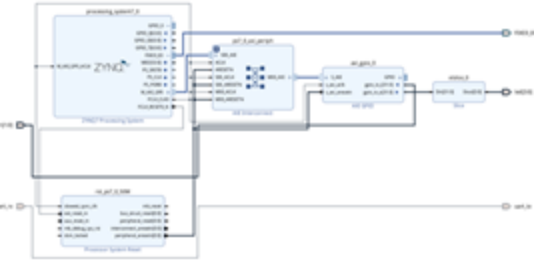
https://pynq.readthedocs.io/en/latest/overlay_design_methodology/pspl_interface.html

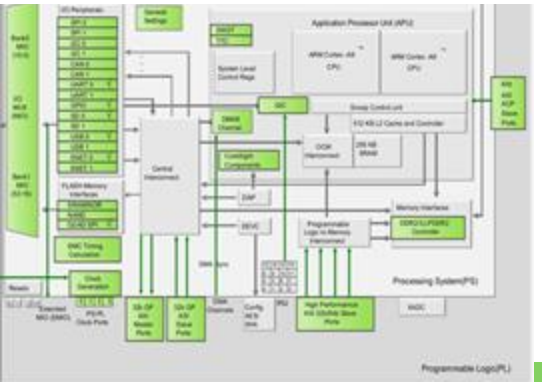
FPGA fabric,
HDMI/ETH/LED/…

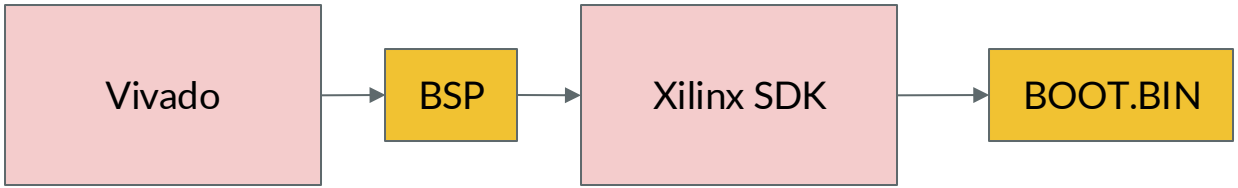
Custom Logic
bitstream

Are you confident…

- Building a Zynq BOOT.BIN firmware by yourself?
- How long does it take?







.bit

PL Bitstream
PS Configuration

ps7_init.c
xparameters.h

FSBL
User App

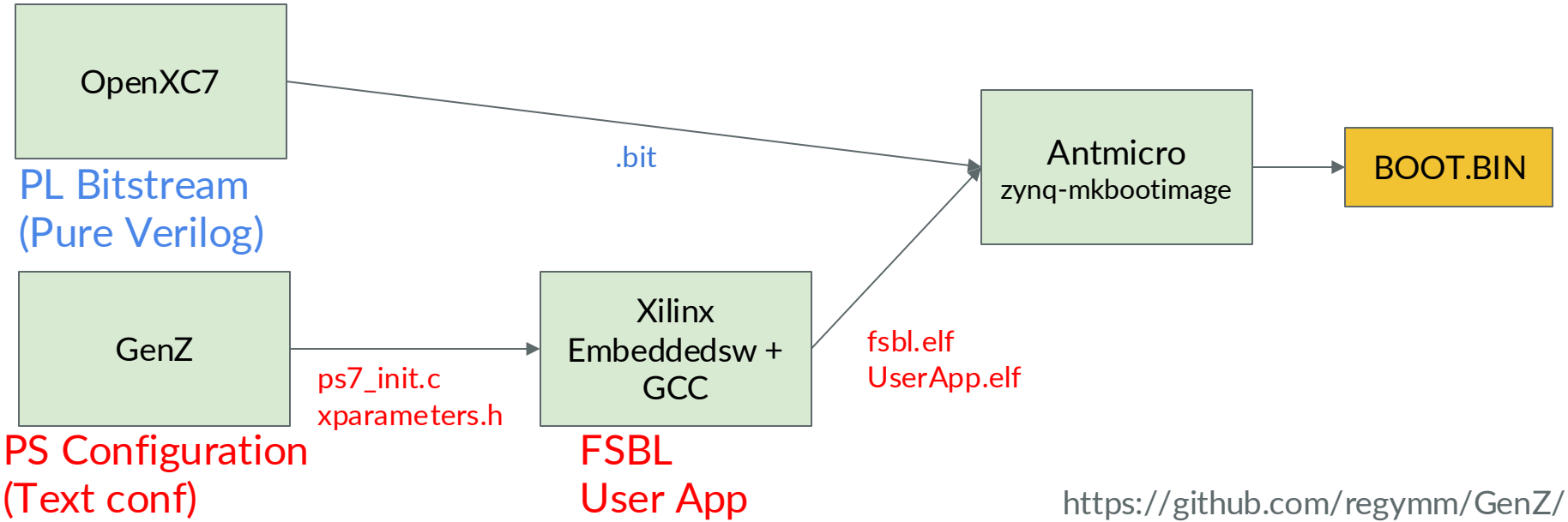
.bit

fsbl.elf
UserApp.elf

Hundreds of mouse clicks!

OpenXC7 + GenZ

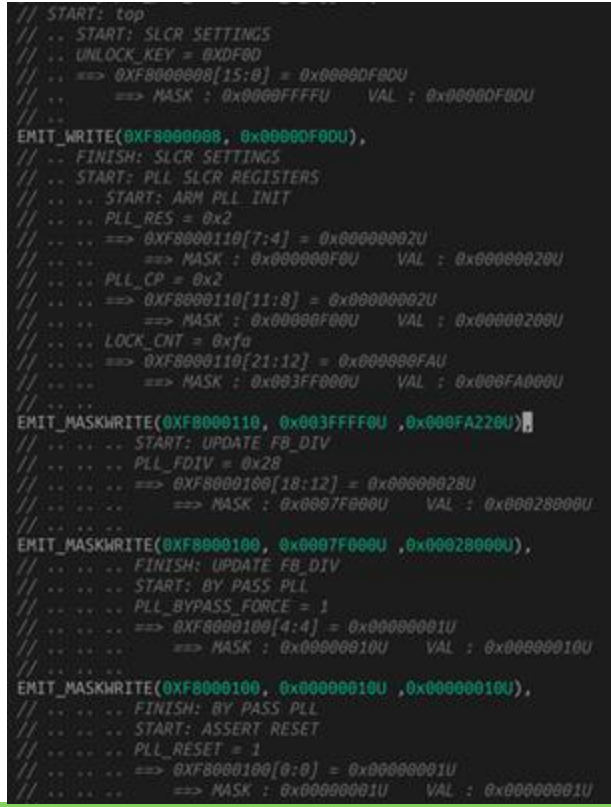
- BOOT.BIN in **5 minutes**
- Awesome through 2035



https://github.com/regymm/GenZ/

Decoding the ARM registers

- 100+ reg writes
- Zynq 7000 SoC Technical Reference Manual (UG585)
  - PLLs (APU, DDR, IO)
  - Clock Freqs (APU, DDR, every peripheral)
  - DDR (TODO)
  - MIO (MUX selection)
  - PERIPH (every peripheral's register space)
  - Debug (???)



What does this mean?

Enjoy RP2040? How about Zynq!

	RP2040	**Zynq 7010**
“PS”	2x Cortex M0+ @ 133 MHz 264 kB SRAM UART, SPI, etc USB 1.1 	2x Cortex A9 @ 667 MHz 256 kB OCM + DDR UART, SPI, SDCARD, etc USB 2.0, 1Gbps ETH 
“PL”	8x Programmable I/Os Modules	28K+ LE
I/O	30 GPIOs	80+ HR I/Os
Price	<€5	€10 - €200
Toolchain	**Cross platform, FOSS** pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	**x86 Win/Linux only, Proprietary** Vivado HLx 2019.1: All OS installer Single-File Download (TAR/GZIP - 21.39 GB) **U.S. Government Export Approval**

Enjoy RP2040? How about Zynq!

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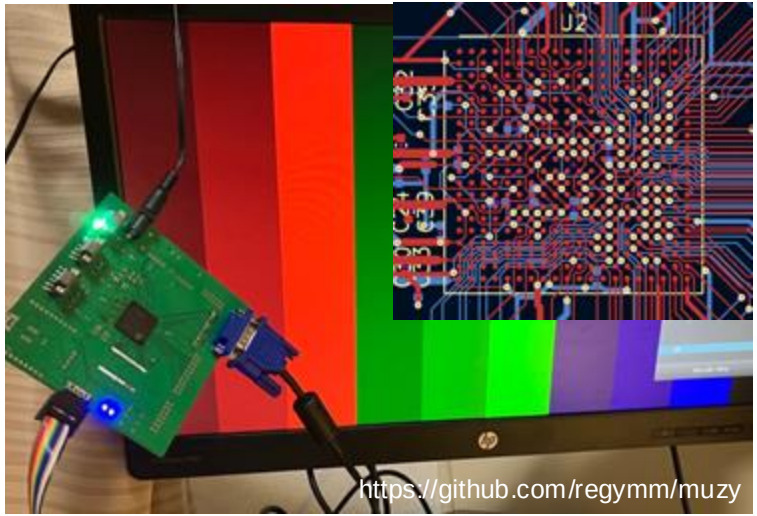
Price	<€5	€10, €60 - €200
Toolchain	**Cross platform, FOSS** pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	**Cross platform, FOSS** **docker pull regymm/openxc7** **git clone https://.../GenZ**

Zynq-as-MCU

- Boards are available
- Upcycled boards set price at **€10**

EBAZ4205, ~€10



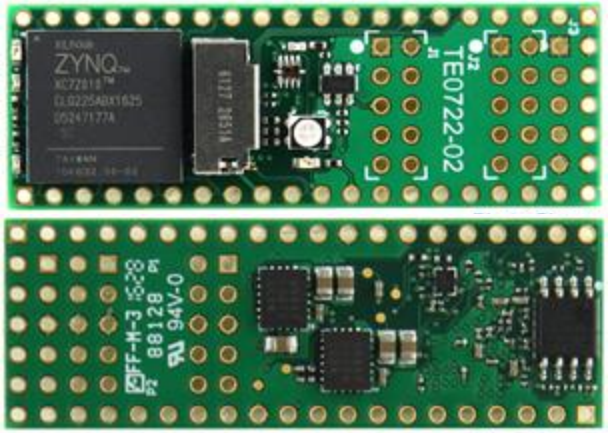
2-Layer
640x480 VGA
115 MHz SDRAM

Muzy-2, BoM ~€10

shop.trenz-electronic.de

Photo Shows Similar Product

ZynqBerryZero, ~€100
Trenz electronic



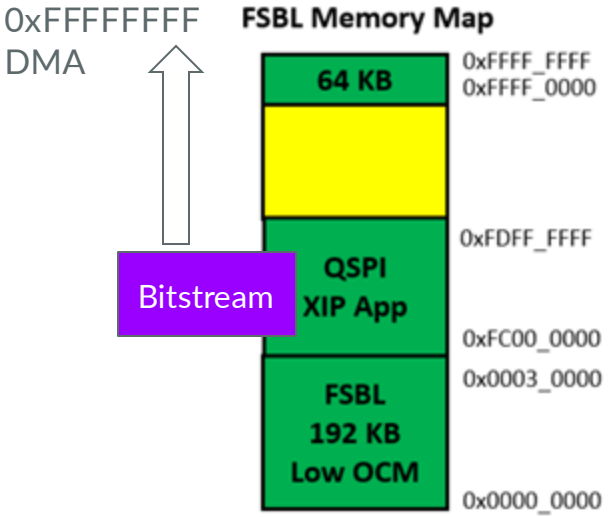
shop.trenz-electronic.de

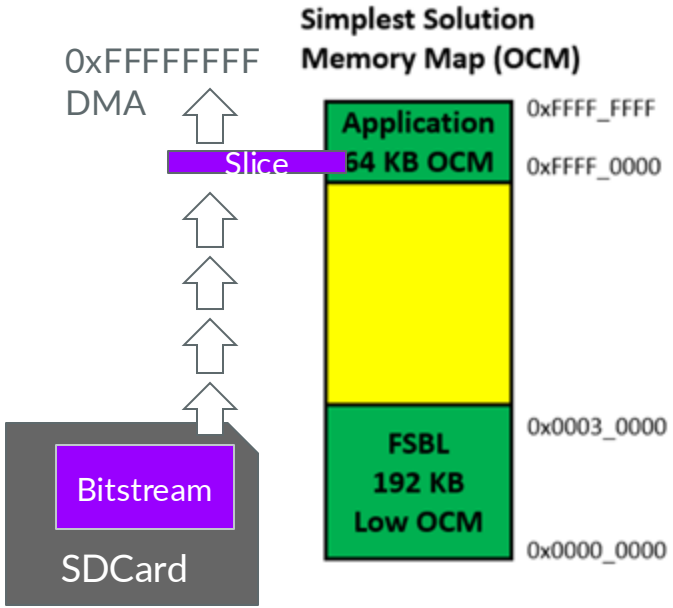
Photo Shows Similar Product

DIPFORTy1, ~€60
Trenz electronic

Possibilities unlocked

- **#1 No DDR SD Boot**
  - Not supported officially, *was* not convenient





https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2418900993/Zynq+7000+Tips+and+Tricks

Possibilities unlocked

- **#2 Overclock🔥**
- hz12opensource/libresdr
- GenZ

```
+cpu_mult_template='EMIT_MASKWRITE\(0XF8000100, 0x0007F000U ,0x000XX000U\),'
+cpu_mult_find='\s'"${cpu_mult_template/XX/(..)}"
+ddr_mult_template='EMIT_MASKWRITE\(0XF8000104, 0x0007F000U ,0x000XX000U\),'
+ddr_mult_find='\s'"${ddr_mult_template/XX/(..)}"
```

```
z7000_ps_param_900 = {
    'freq'  : { 'crystal'  : 33.333333333,
                'apu'      : 900.0
              }
}
```

Flexibility meets more flexibility

- **#3 PL bitstream built on PS itself**
- It’s an ARM anyways
- OpenXC7 runs on 1 GB mem

https://www.youtube.com/watch?v=XkAzzpYiAUg

Larger devices

- **Zynq 7030, 7035, 7045, 7100 now supported by OpenXC7**
- Would have transceivers and PCIe blocks, DDR3 on PL, …

Future

Freedom is the future

- PetaLinux?
- SDRs and more

digikey.com

Openwifi

Acknowledgement

OCP-TAP

LUG@USTC

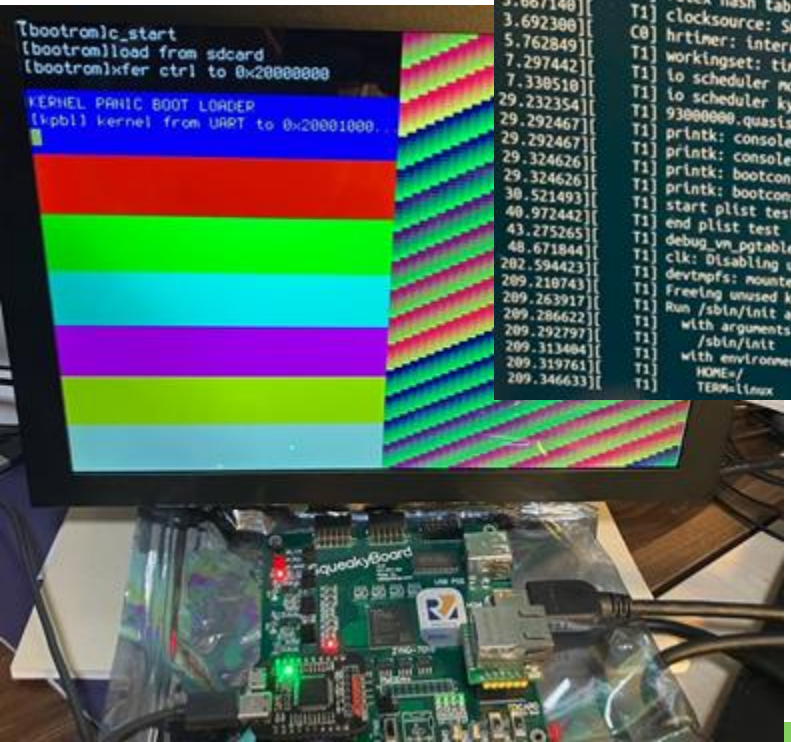
VLAB@USTC

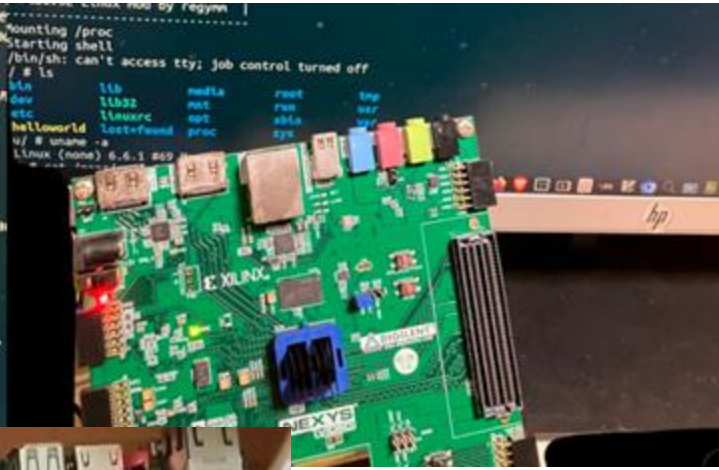
Thank you!

- github.com/regymm
- ustcymgu @ gmail.com

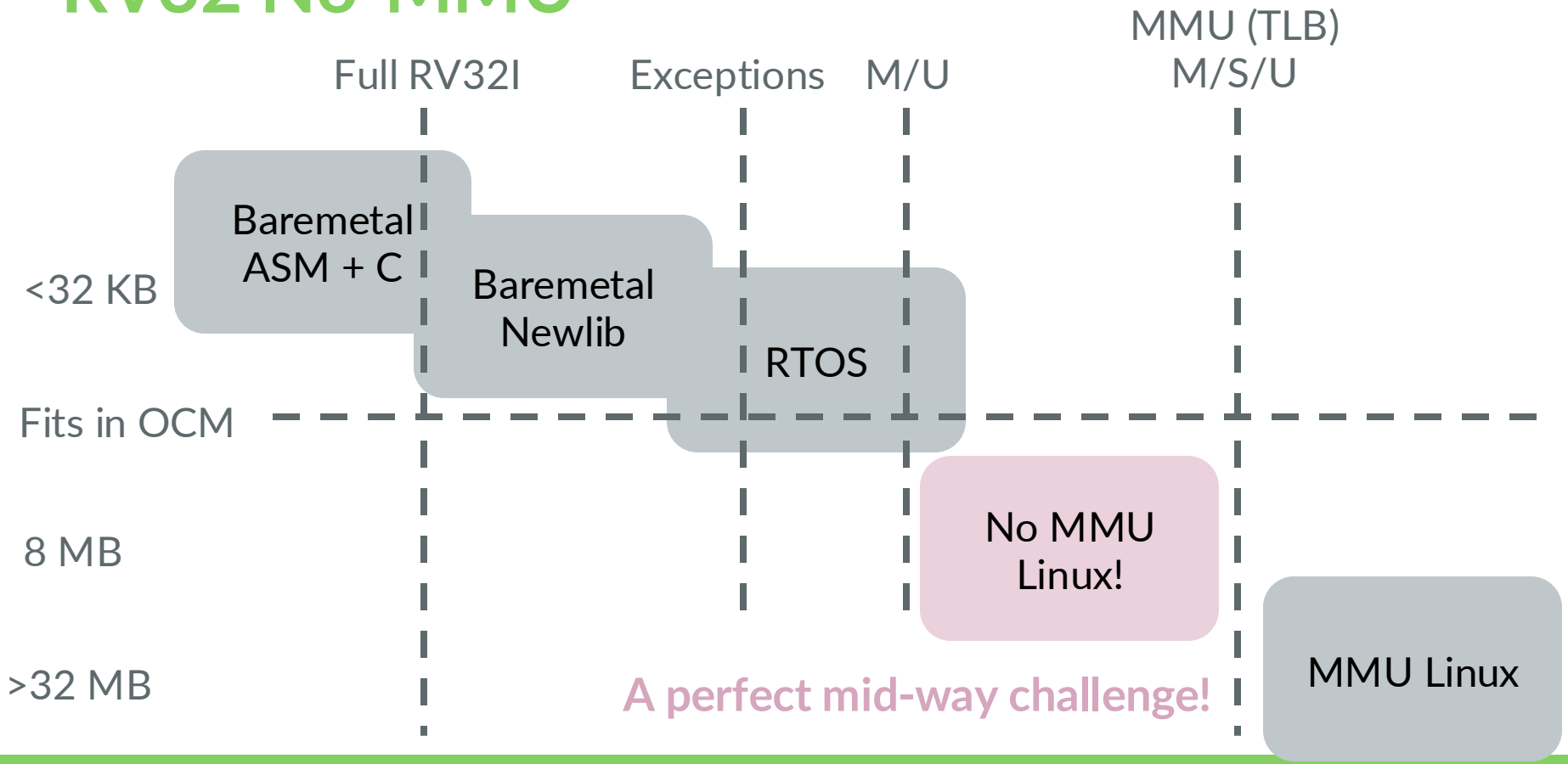
Quasi SoC IRL

(Two cores, one RV32IMA_Zicsr main CPU, one RV32I VT100)





RV32 No-MMU


Full RV32I
Exceptions
M/U
MMU (TLB)
M/S/U
Baremetal
ASM + C
Baremetal
Newlib
RTOS
<32 KB
Fits in OCM
8 MB
>32 MB
No MMU
Linux!
MMU Linux
A perfect mid-way challenge!