How Good is RISC-V:

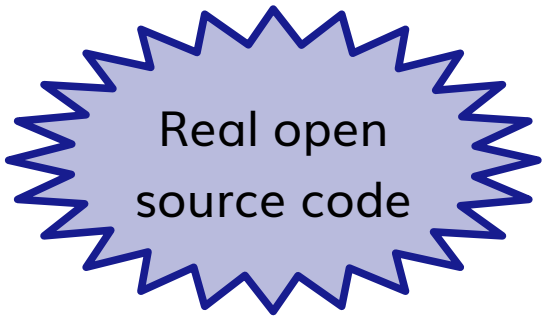
Comparing Benchmark Results

Jeremy Bennett

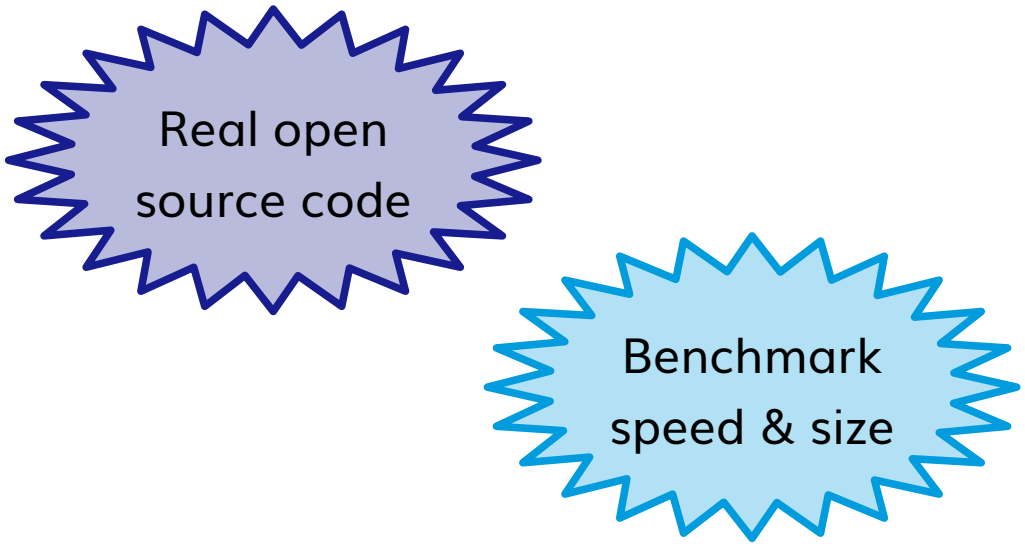
Open Source Benchmarking

How to Benchmark

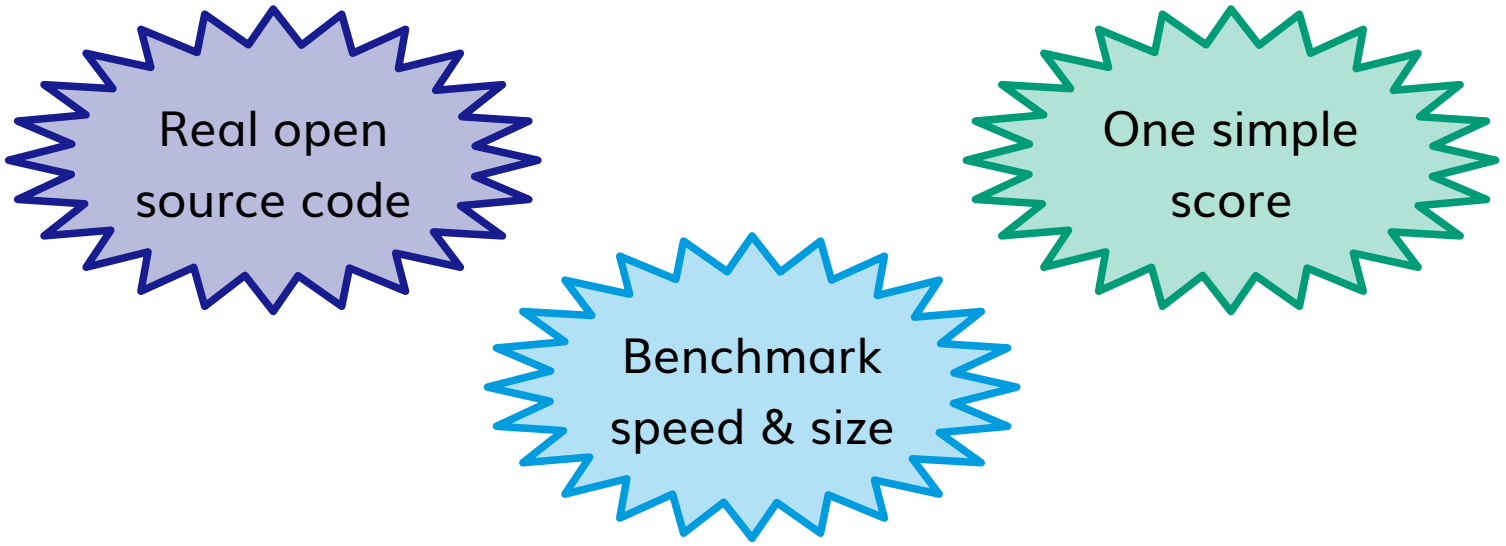
How to Benchmark



How to Benchmark



How to Benchmark



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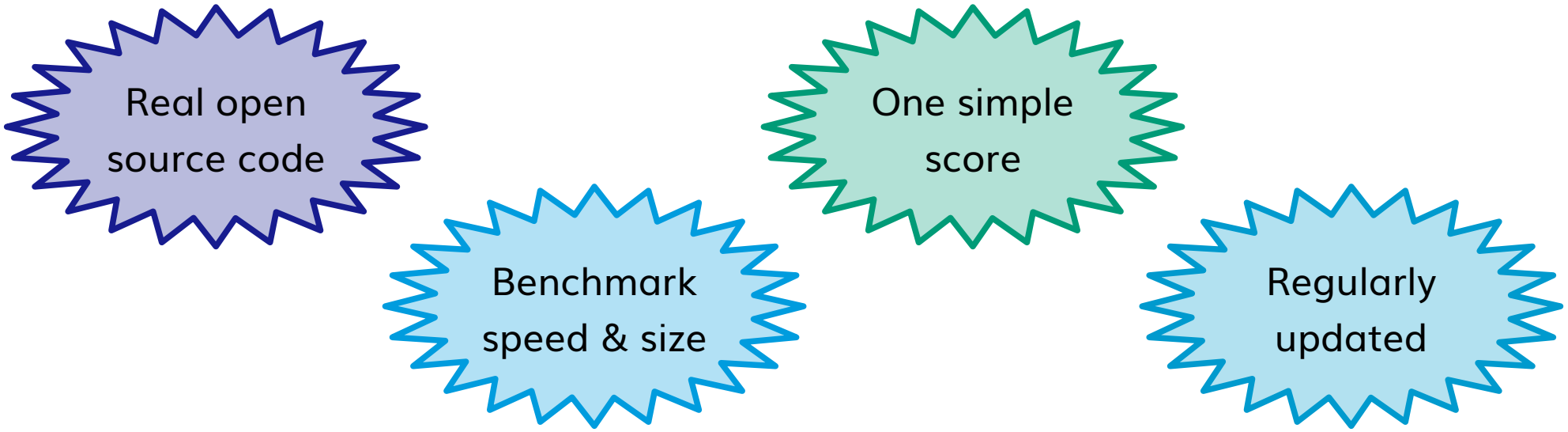

How to Benchmark

Real open source code

One simple score

Benchmark speed & size

Regularly updated

SPEC CPU 2016 & 2017

Application class cores

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One simple score

Benchmark speed & size

Regularly updated

SPEC™

SPEC CPU 2016 & 2017

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Embench

Embench IoT 1.0 & 2.0

Microcontroller cores

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Benchmarking Targets

Benchmarking Targets

RISC-V
CV32E40Pv2 on Nexys A4 FPGA @ 15MHz
HiFive Unmatched @1.4GHz
MILK-V Pioneer @ 2.0GHz
BananaPi BPI_F3 @ 1.6GHz
QEMU User Mode

Benchmarking Targets

RISC-V	Arm
CV32E40Pv2 on Nexys A4 FPGA @ 15MHz	STM32F407 @ 16Mz
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Benchmarking Targets

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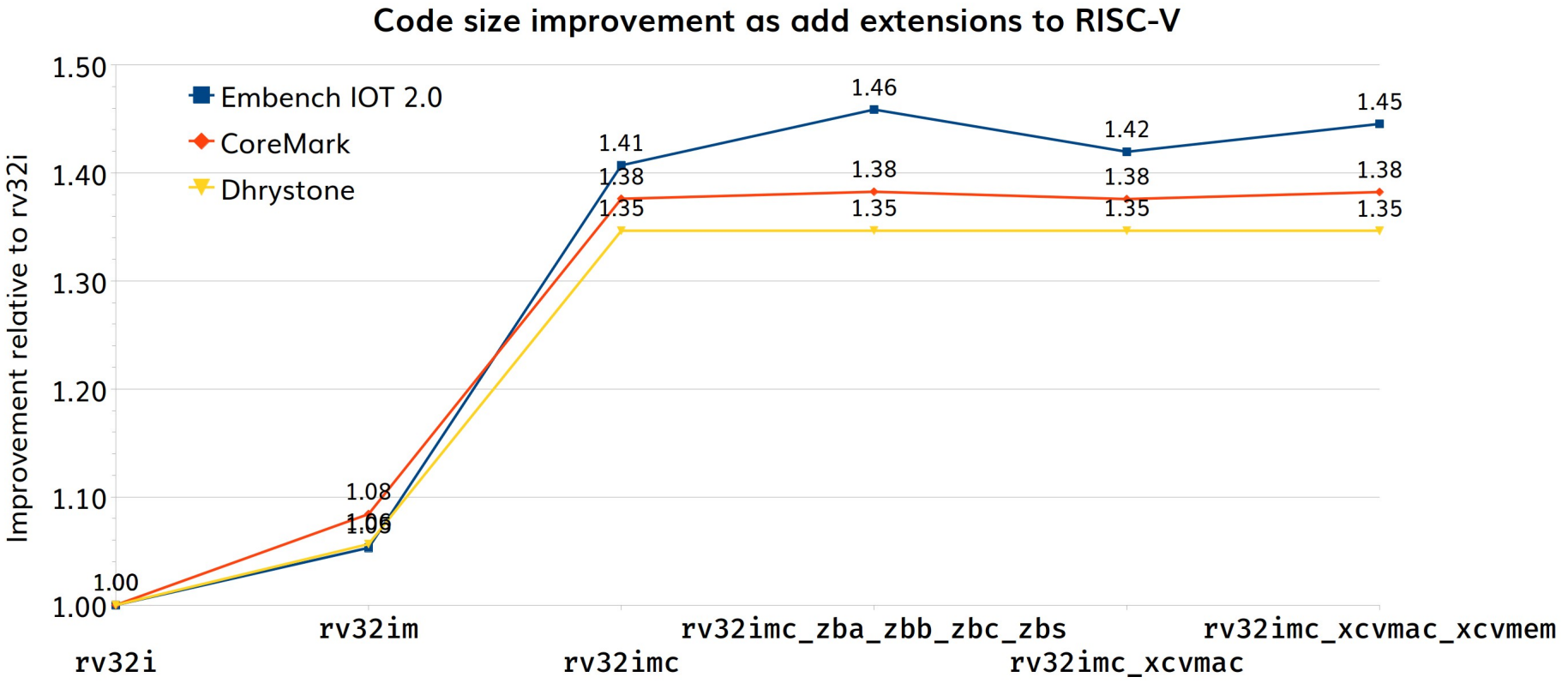
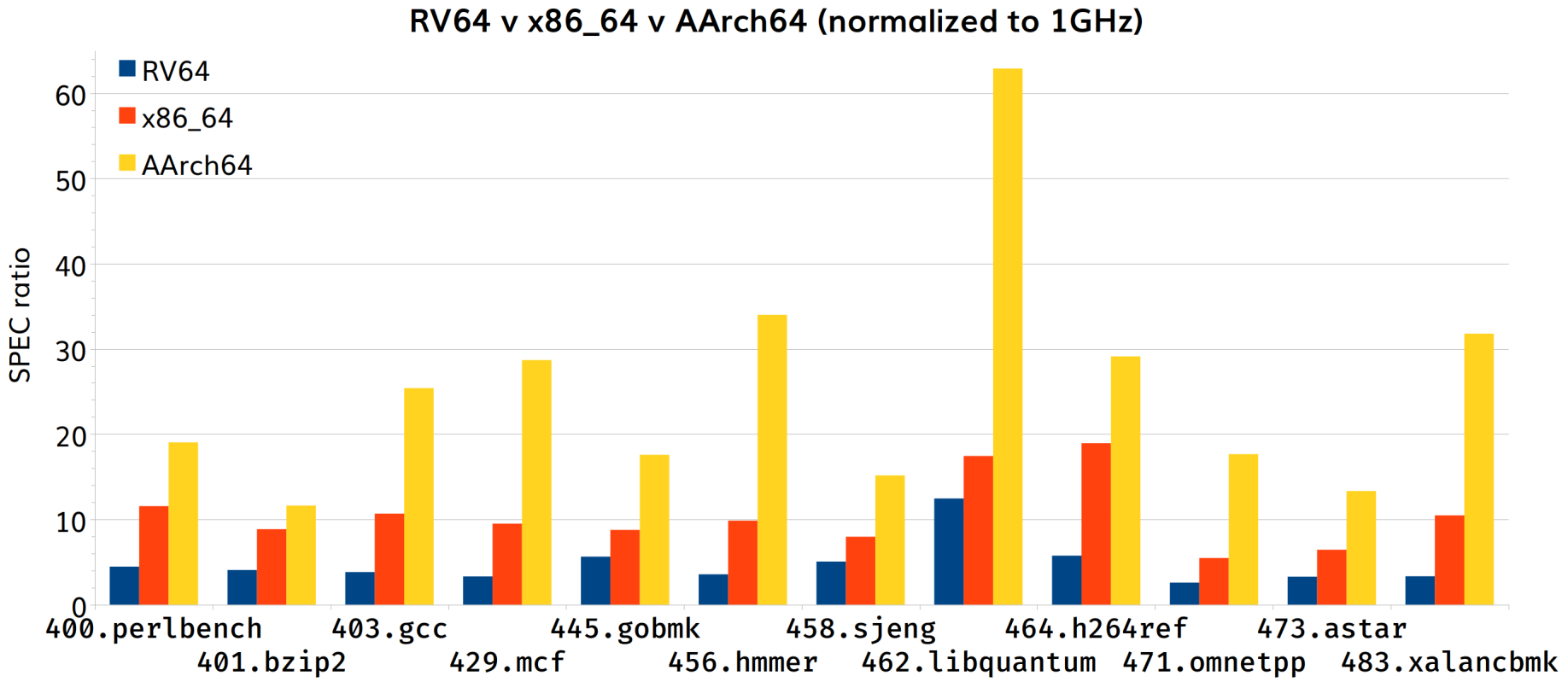
Dhrystone & CoreMark



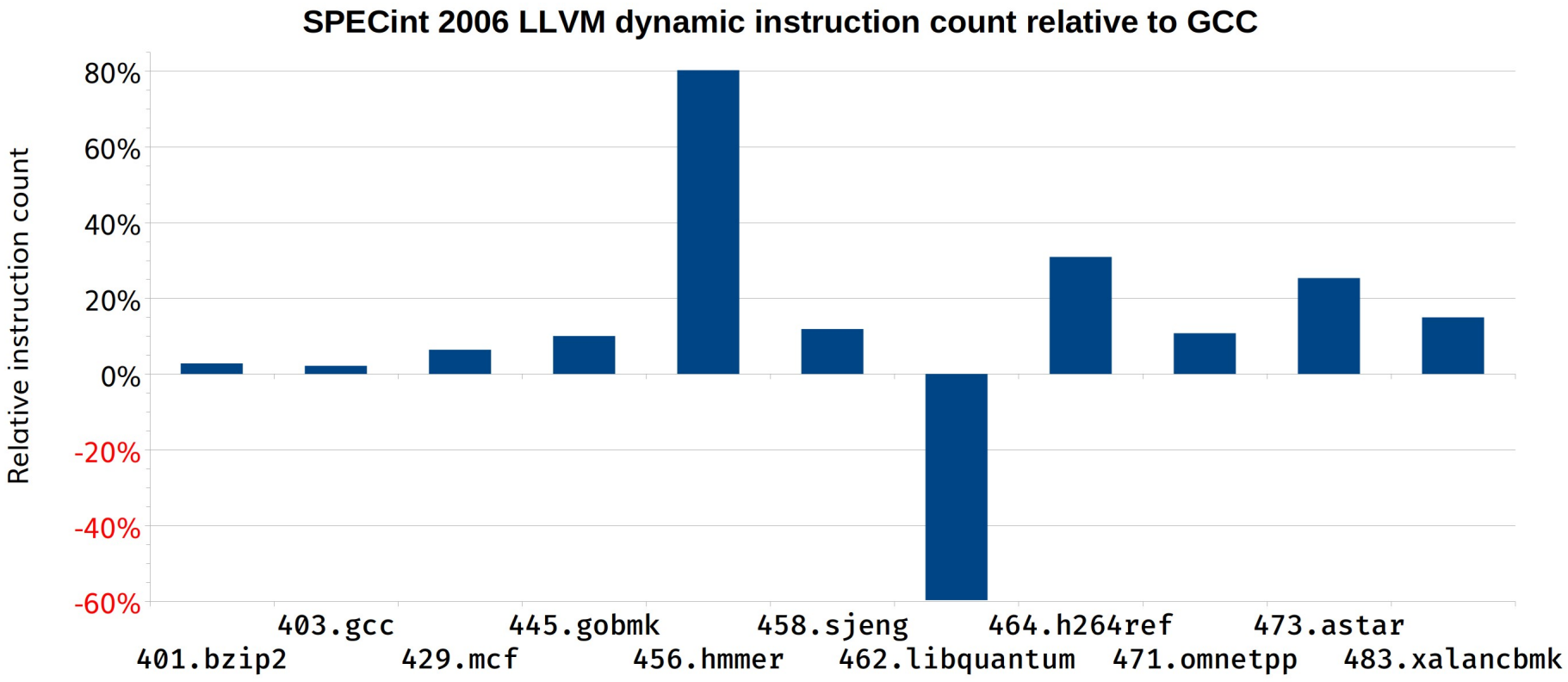
Application Class Processors

SPEC CPU 2006 & 2017

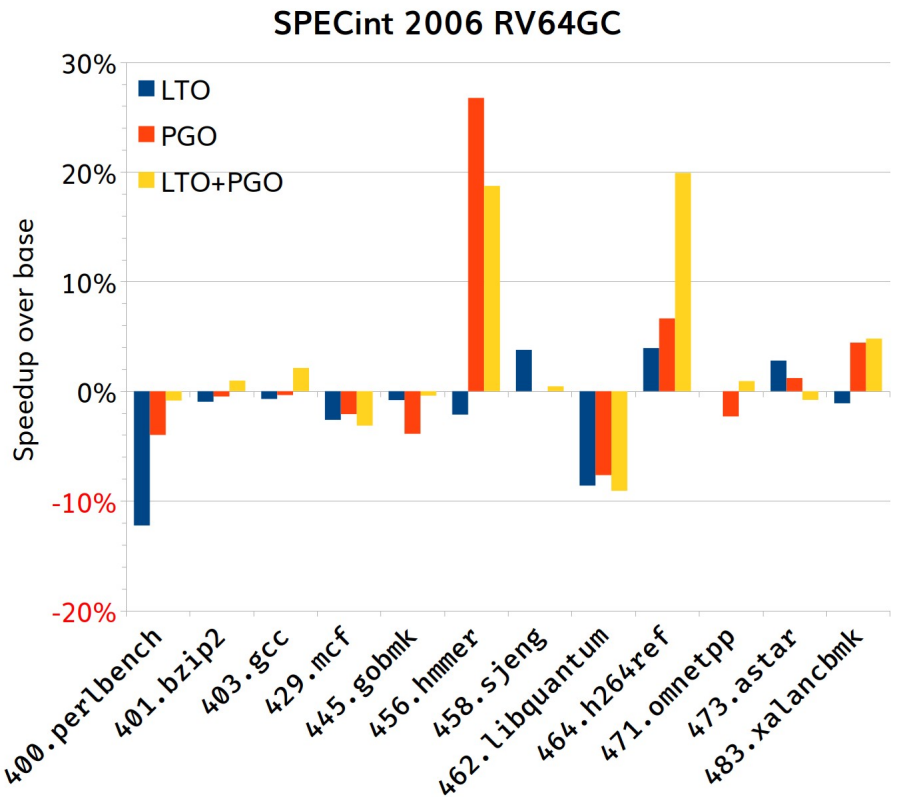
Comparing Architectures (SPEC CPU 2006)



GCC v LLVM



Impact of LTO and PGO



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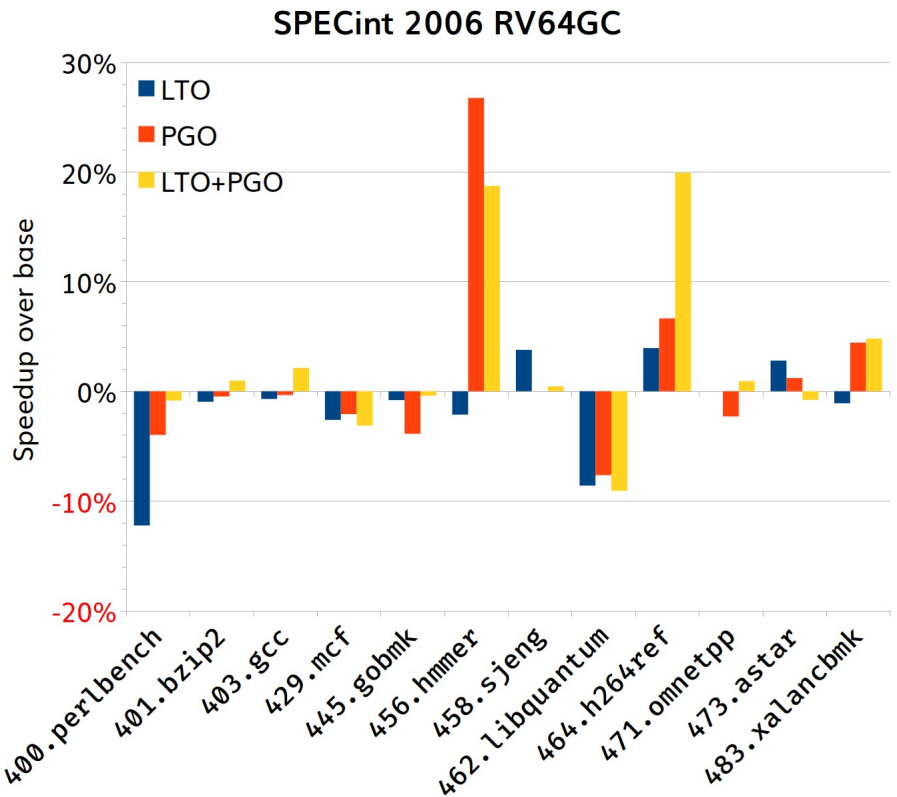
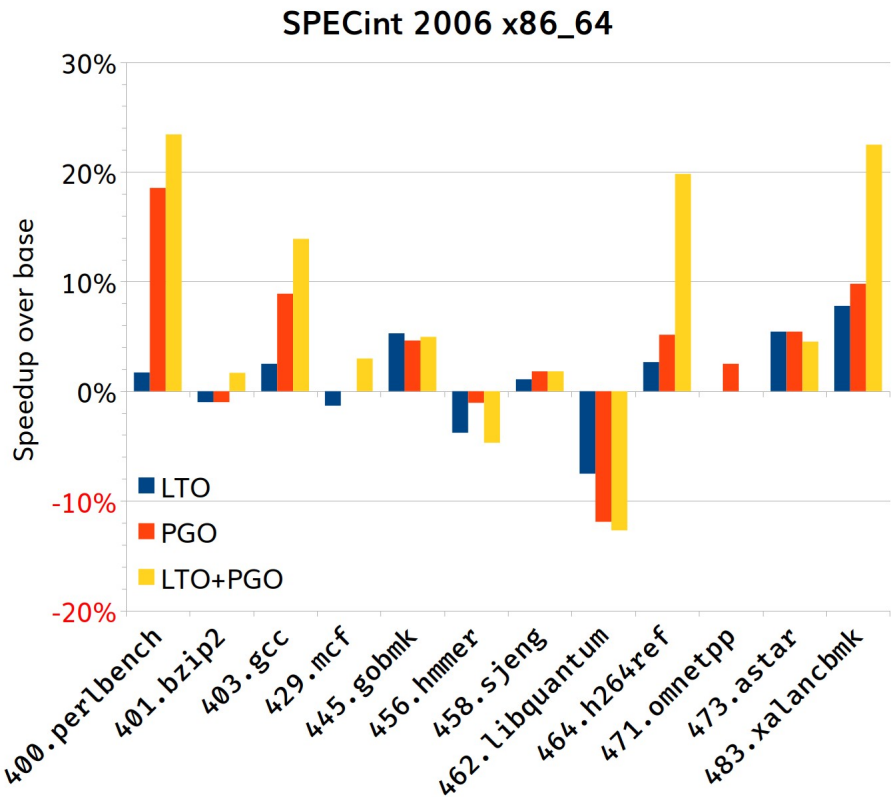
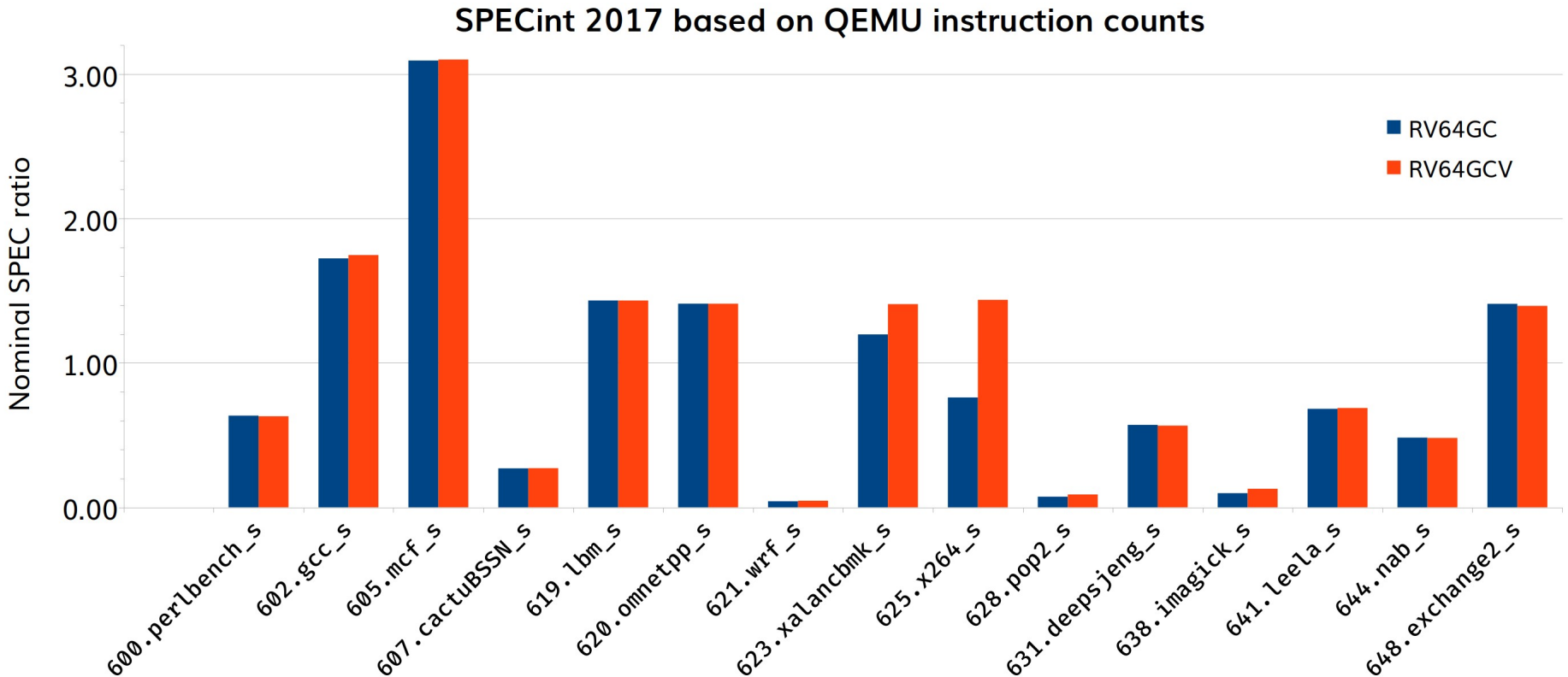




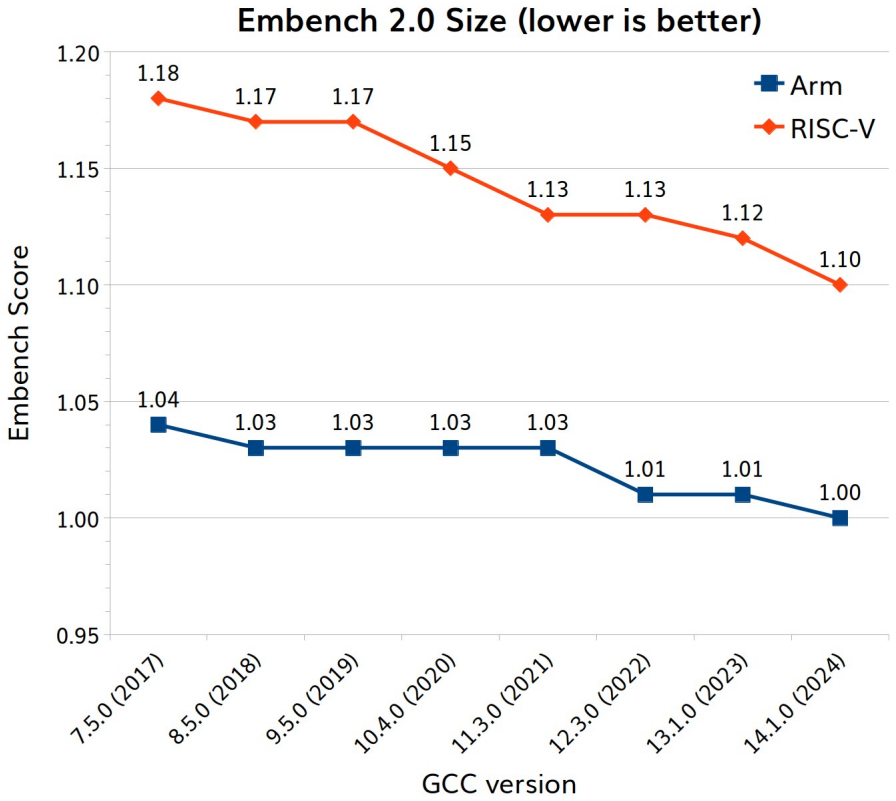
RISC-V Vector (RVV)



Microcontrollers

Embench IoT 1.0 and 2.0

Compilers over Time (GCC)



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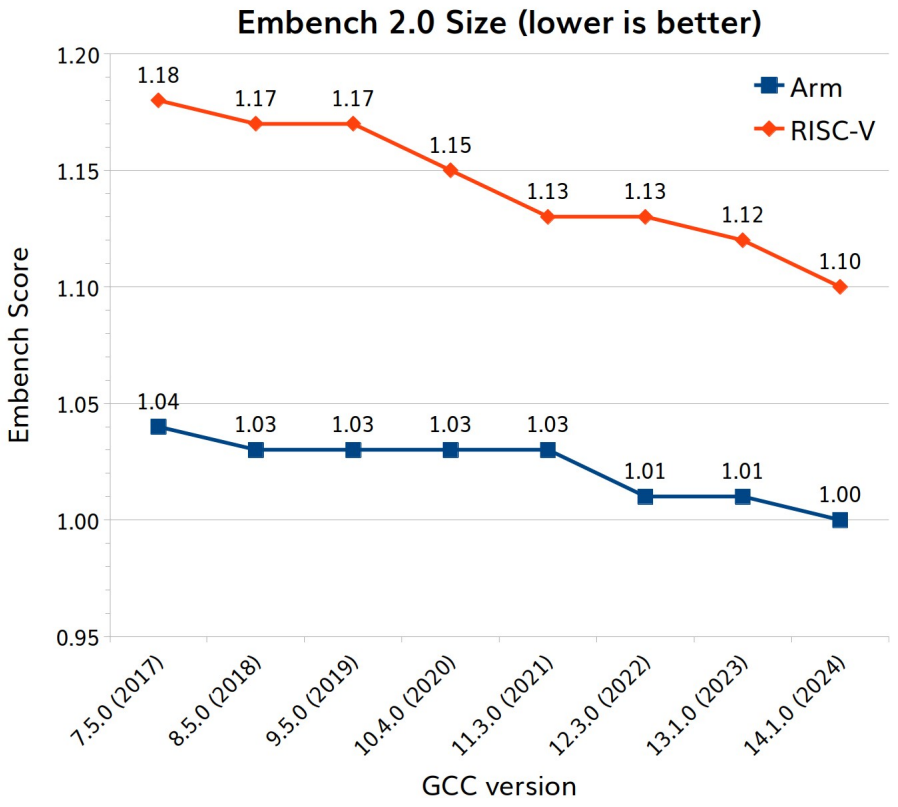
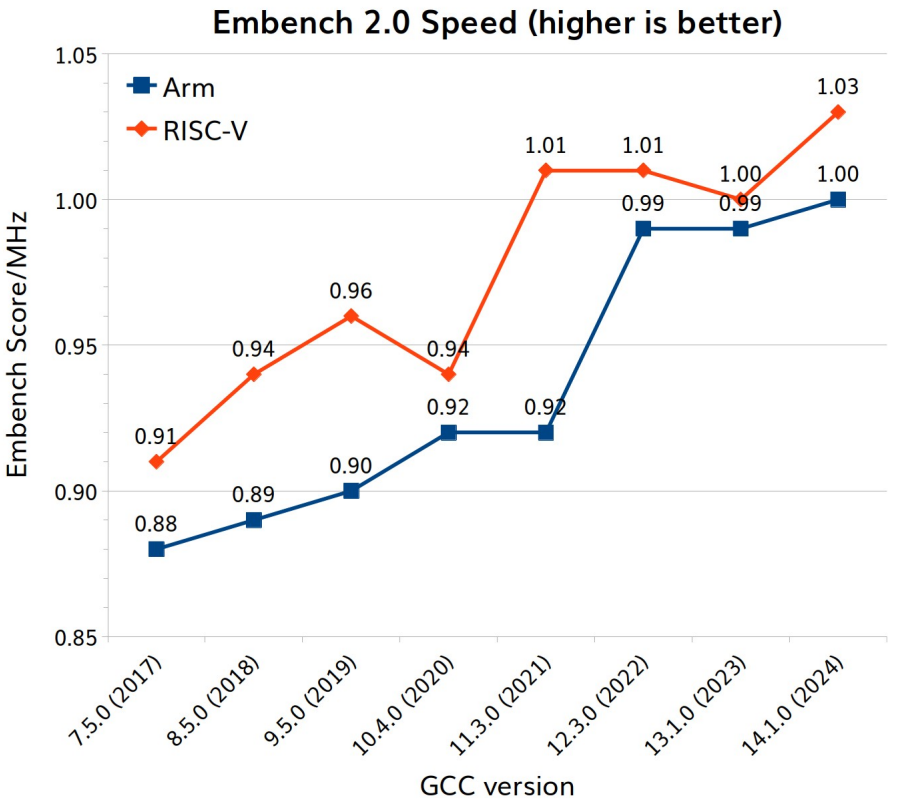
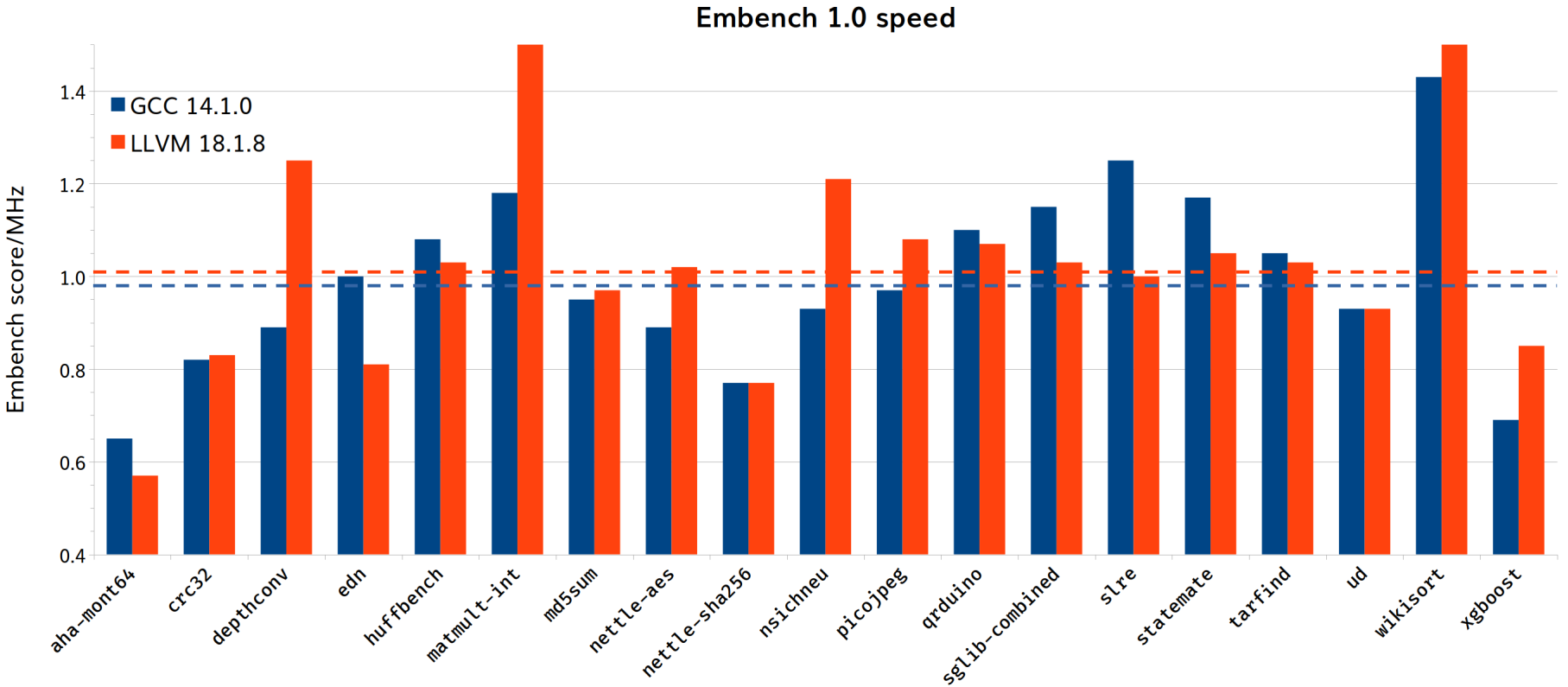
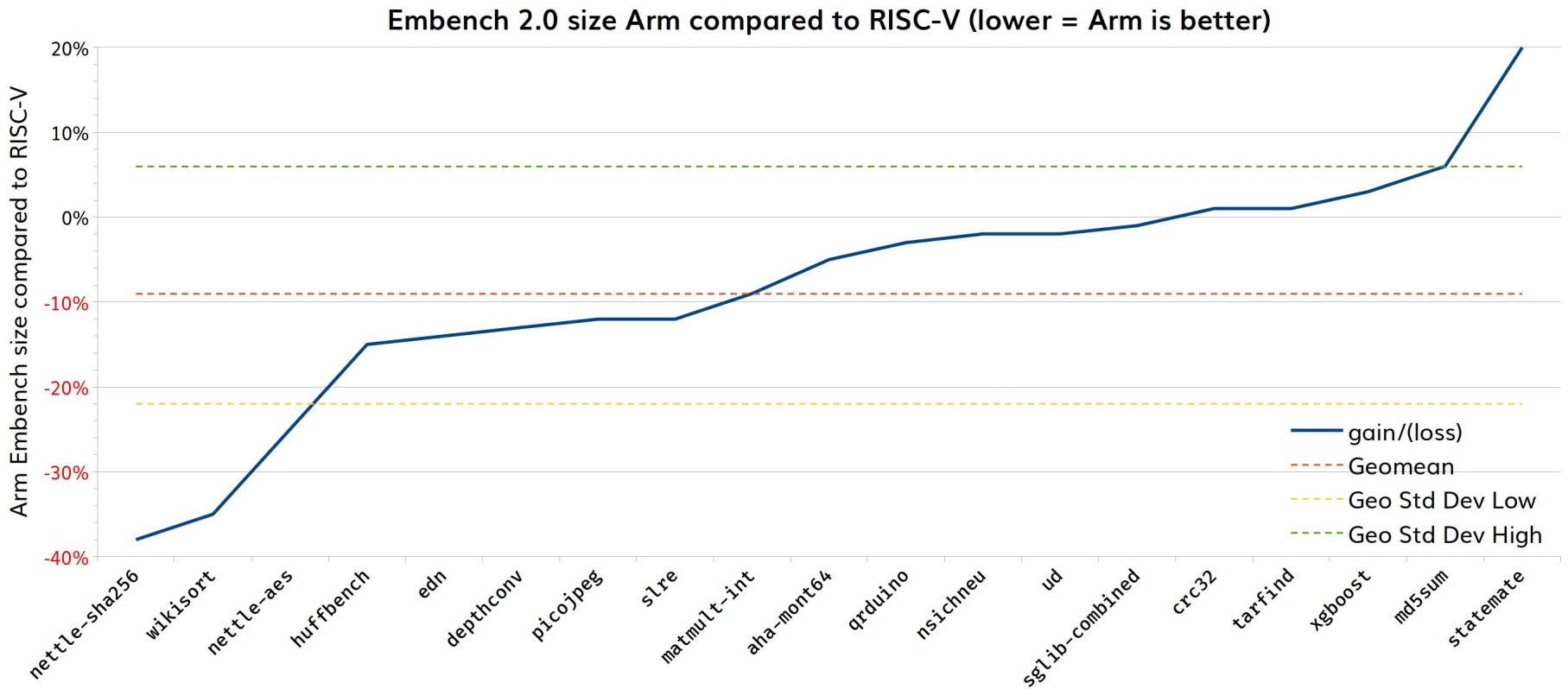




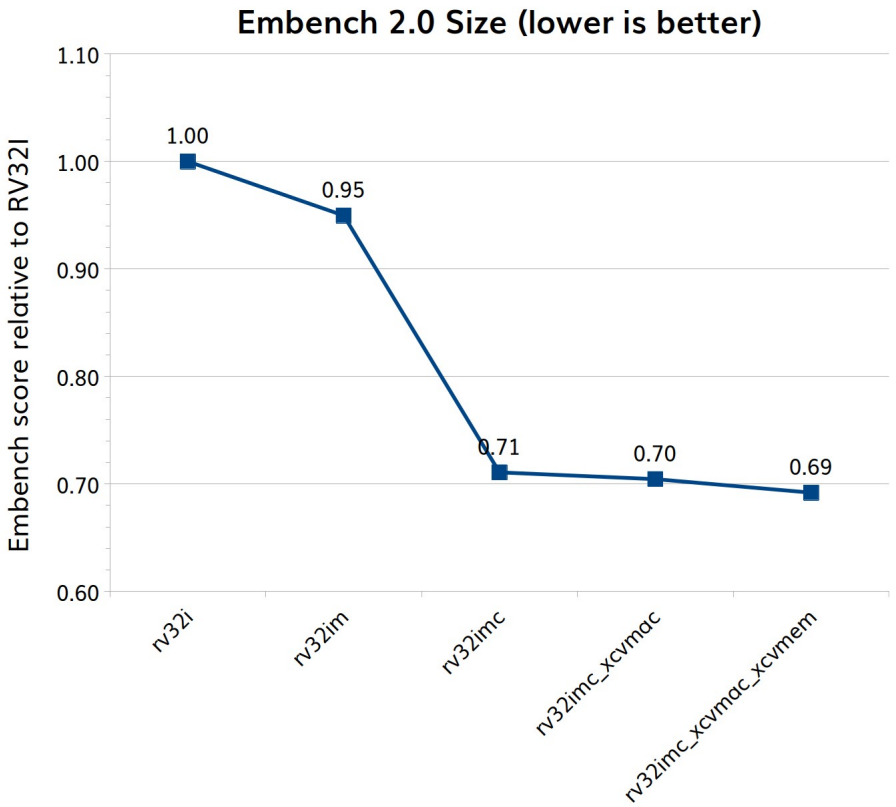
Comparing Compilers



Comparing Architectures



Impact of ISA Extensions



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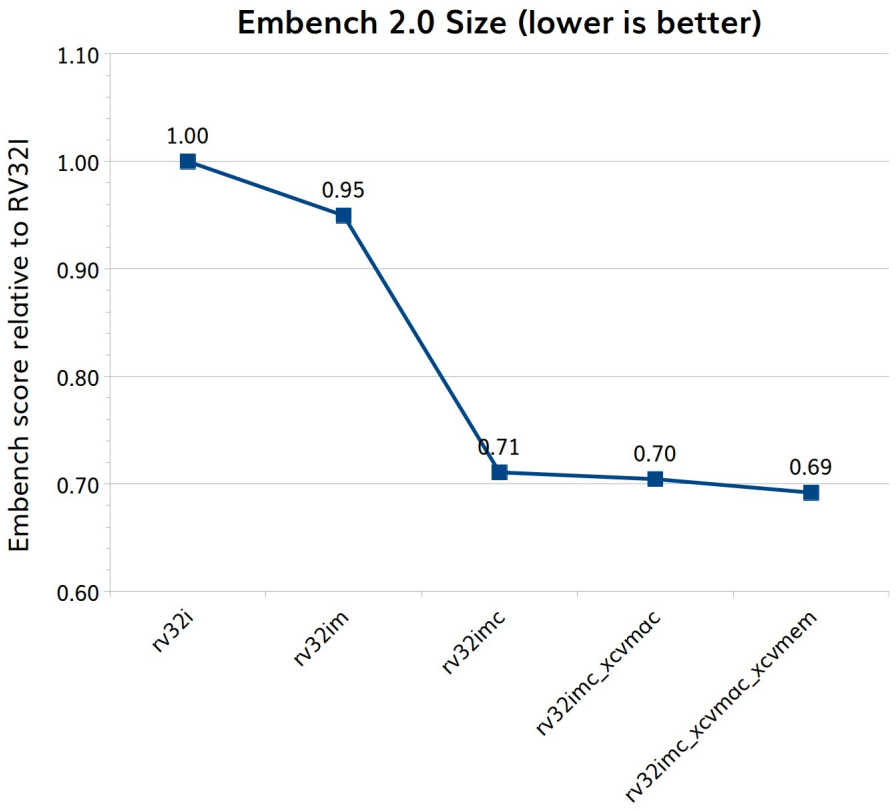

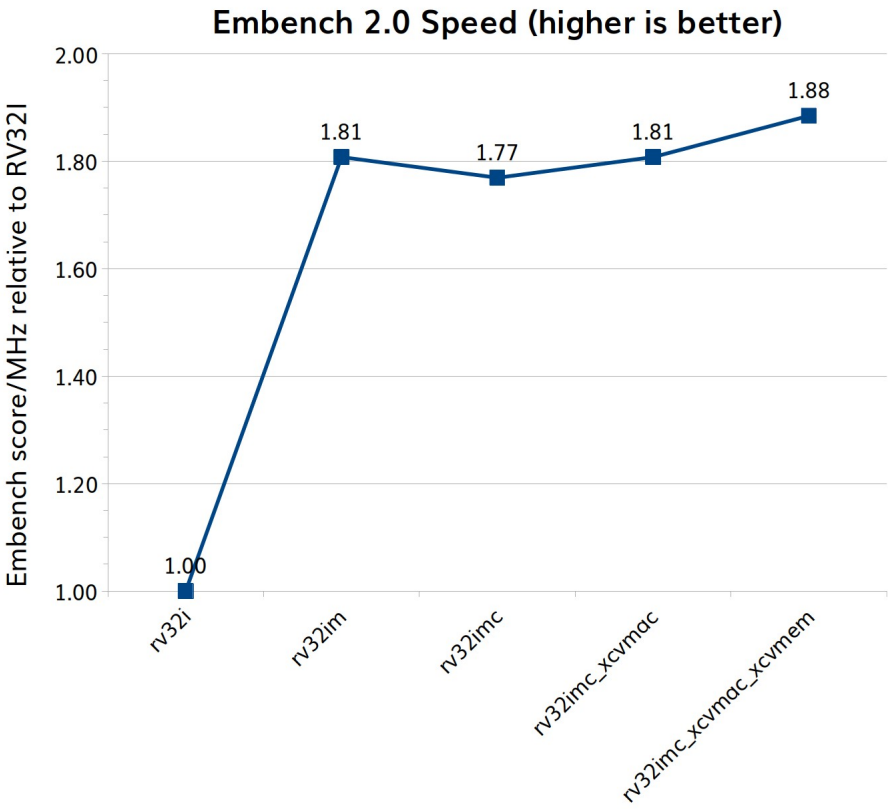

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The Compiler Community

Community Statistics

Metric	RISC-V	Arm
# commits	1,058	611
# committers	45	43
Most commits	363	173
# committers to reach 90%	15	13
# companies committing	16	12

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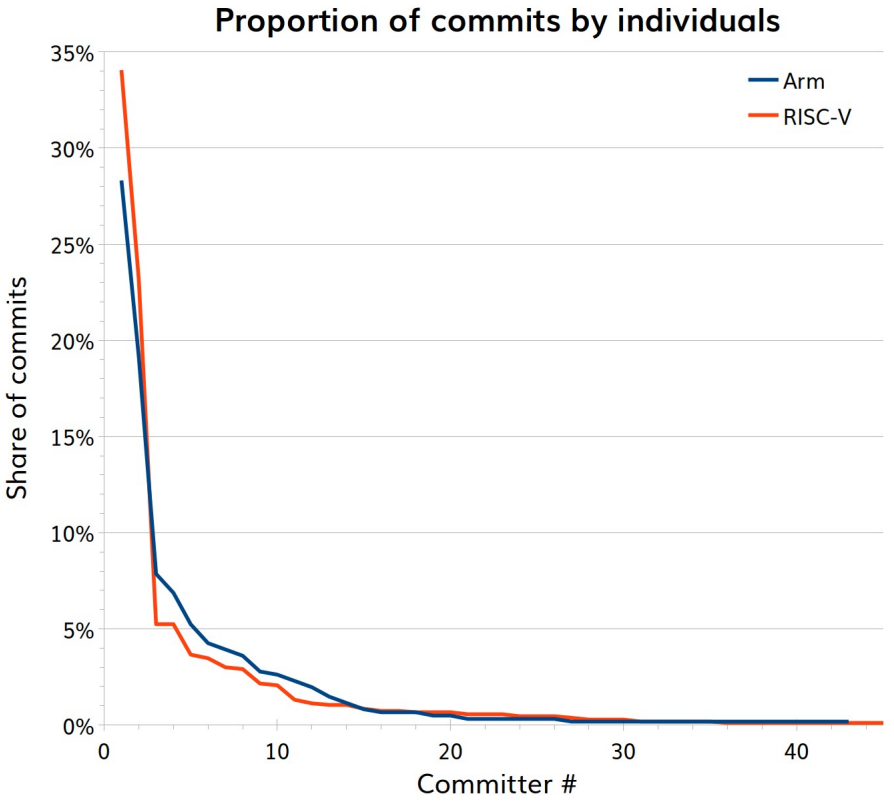

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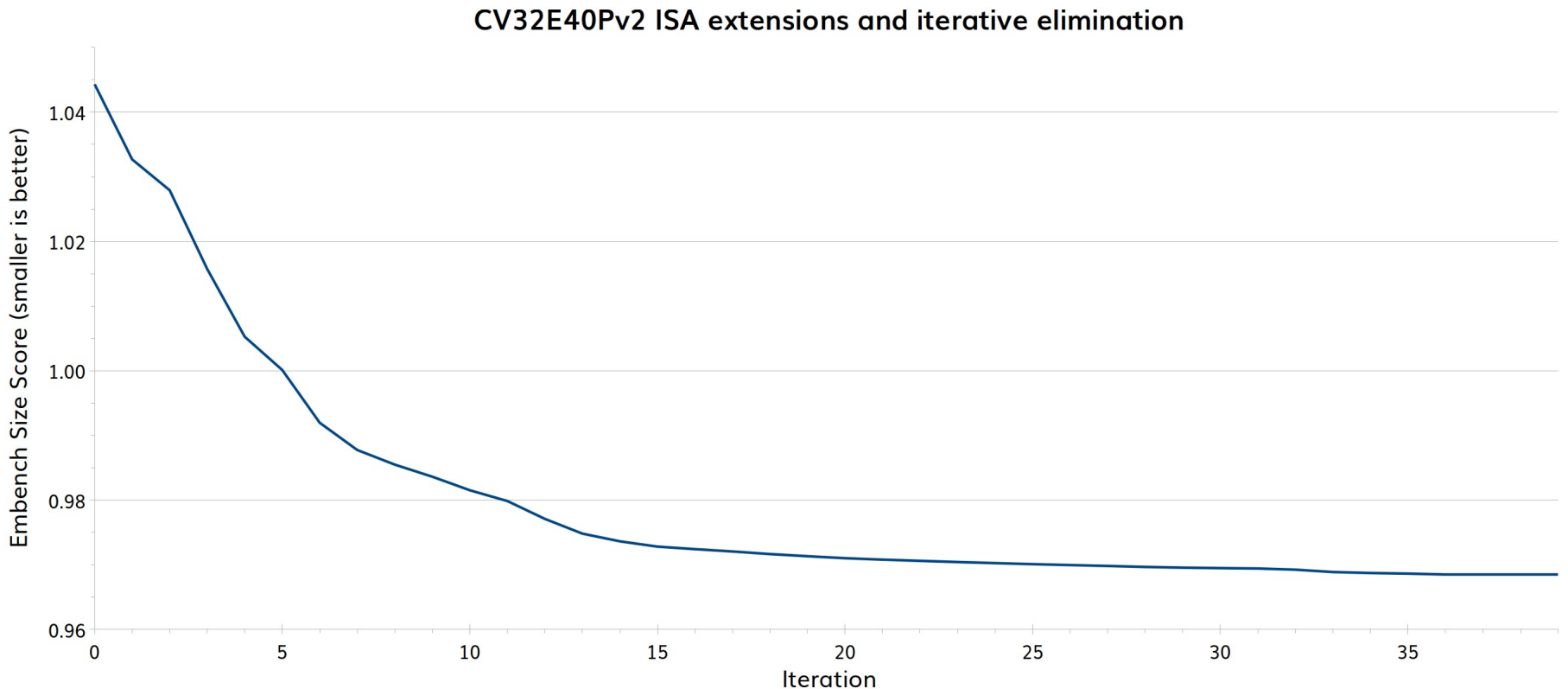
Using Benchmarks:

Improving the Compiler

Iterative and Combined Elimination



Acknowlegements

Dave Patterson and the Embench community

The Open Hardware Foundation

The GCC and LLVM commuities

The Embecosm team

Thank You

jeremy.bennett@embecosm.com

embecosm.com