FOSDEM'25
Brussels / 1 & 2 February 2025

The IHP OpenPDK Initiative

Status and RoadMap

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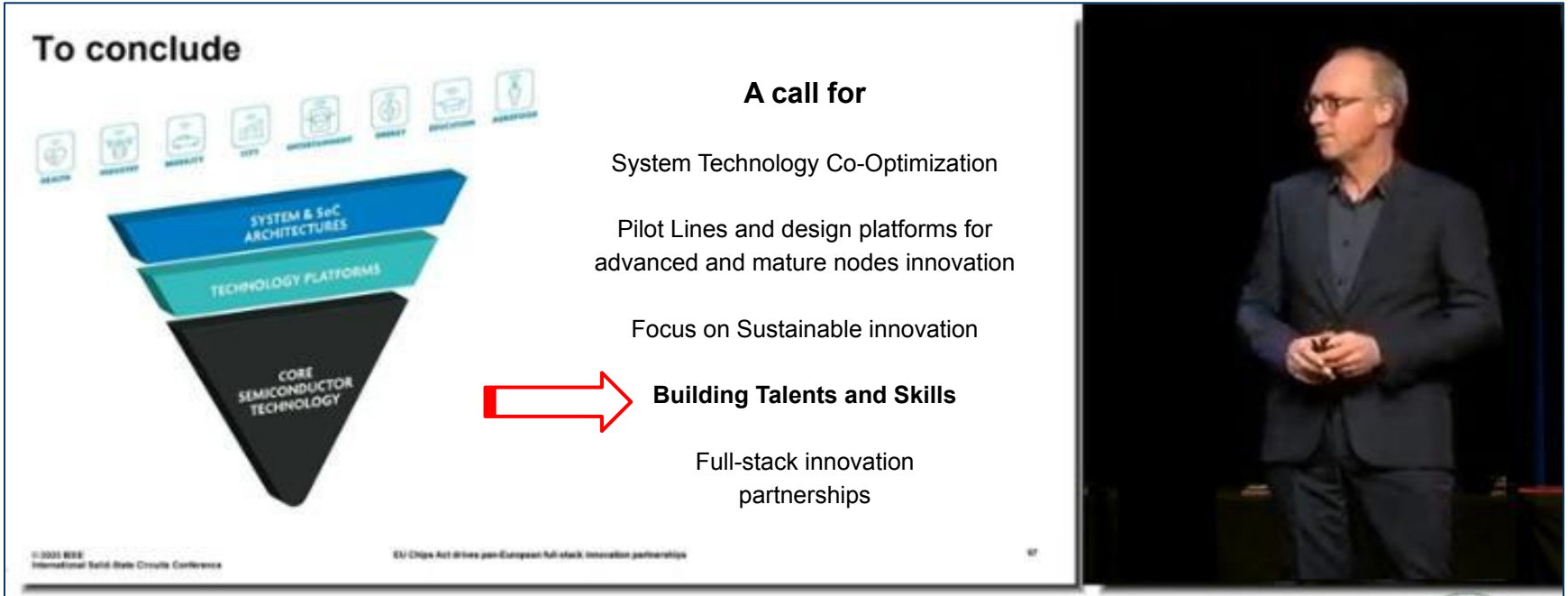
The IHP OpenPDK Initiative
Status and RoadMap

Outline:

- Motivation
  - Talent Gap by job profile in EU
- eSim FOSSEE Tool for IC Design
- Open PDK Initiative
  - SkyWater (US), GF (US), AIST ACPS (J), IHP (D)
- IHP Open PDK and FOSS EDA/CAD Tools Flow Development
- What's next?
  - Open PDK to Empower Researchers and IC Designers
  - Roadmap for Open-Source EDA in Europe
- Acknowledgment

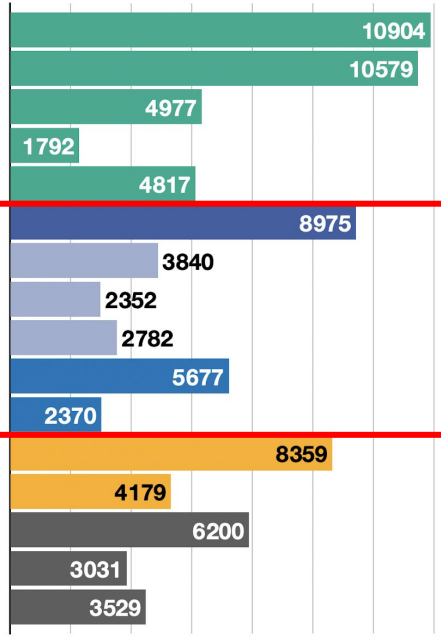
Motivation: A call for Building Talent and Skills



[REF] EU Chips Act Drives Pan-European Full-Stack Innovation Partnerships
Plenary Session at ISSCC, FEB.20, 2023
Jo De Boeck, Executive VP and CSO, imec and KU Leuven, Belgium

Talent Gap by job profile in EU by 2030

Field	Semiconductor workforce shortage in the EU from 2024 to 2030		% total	Per year
	TOTAL workforce shortage	75387	100 %	12565
Manufacturing (33 000)	**Process technicians**	10904	14 %	1817
	Process engineers	10579	14 %	1763
	Maintenance technicians	4977	7 %	829
	Operator / quality inspector technicians	1792	2 %	299
	Others (Automation, materials, quality / reliability)	4817	6 %	803
Design (9 000)	**Design engineers**	8975	12 %	1496
	Of which system designers	3840	5 %	640
	Of which analog designers	2352	3 %	392
	Others (digital, layout, simulation enablement)	2782	4 %	464
Test (8 000)	**Test engineers** (test, verification, characterization)	5677	8 %	946
	Test technicians	2370	3 %	395
ICT (12 500)	**Software engineers**	8359	11 %	1393
	Data specialists	4179	6 %	697
Application engineers		6200	8 %	1033
Experts in cybersecurity (by design, secure HW)		3031	4 %	505
Other technical positions (Sustainability, etc.)		3529	5 %	588



Design and cybersecurity profiles ranked as the **most challenging** to fill.

The issue is twofold:

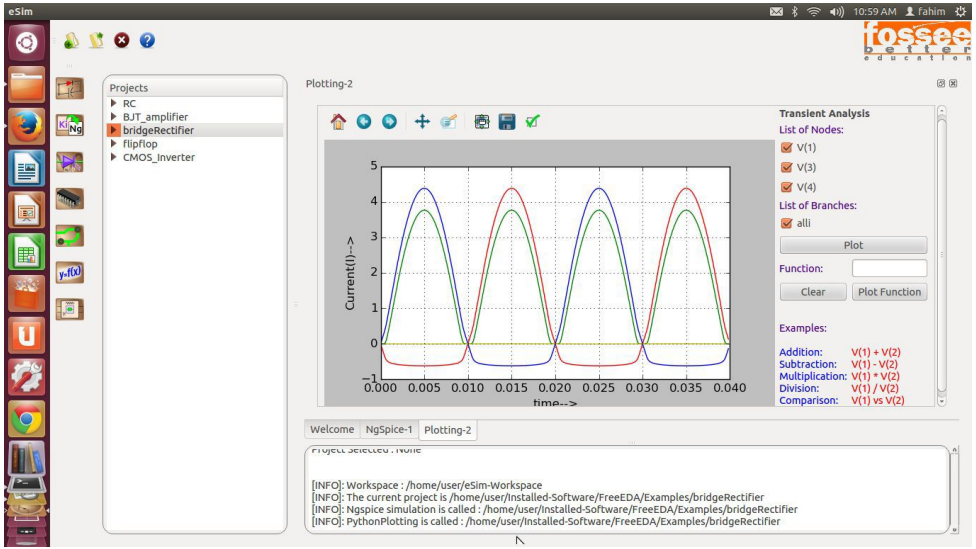
- **Lack of training** capacities / interest (especially electrical engineering)
- **Lack of interest** from students in STEM that prefer ICT studies.

EUROPEAN CHIPS SKILLS ACADEMY

Co-funded by the European Union

[REF] DECISION Etudes & Conseil, European Chips Skills Academy (Dec.2024)
(Only long-term needs, not considering the workforce needed to build the fabs)

eSim **FOSSEE** Tool for IC Design



- **Collaborative effort**
  - A **global advisory committee** for eSim to connect industry and academia.
  - Reaching out to organizations globally for partnerships.
  - **eSim Team participated in the WOSET conference**, showcasing advancements.
  - **eSim Research Migration Initiative** started to shift research papers published using proprietary tools to the **Open Source domain** with eSim.
  - Collaboration with **Open Source Fabs** to enhance hardware accessibility.
  - **Mixed Signal Circuit Design Competition** conducted earlier with Google SkyWater and around 10 designs sent to Efabless Corporation for fabrication as an outcome.

[REF] https://esim.fossee.in/home

Open PDK Initiative

efabless.com

skywater TECHNOLOGY

GlobalFoundries™

Sponsored by Google

The Open-Source FPGA Foundation offers a set of free and open-source tools enabling fast prototyping for FPGA chips and automated EDA support, through open standard collaboration https://osfpga.org/about-us/

- **Semiconductor R&D**: Tapeout of a design is one of the most important aspects of academic semiconductor research and development.
- **Prohibitive cost**: The prohibitive cost of tapeout and complications therein has prevented the majority of R&D folks and startups from participating.
- **Open-Source**: Open PDK Initiative plans to promote and facilitate the usage of open source FPGA technologies.
- **Free tapeouts**: Open PDK Initiative plans to offer a very simple flow for tapeout, and several of those will be free or at minimal costs.

Available Resources:

- SkyWater Open 130nm CMOS PDK: https://github.com/google/skywater-pdk
- OpenLane RTL2GDS Compiler: https://github.com/efabless/openlane
- Caravel Harness: https://github.com/efabless/caravel
- Caravel User Project: https://github.com/efabless/caravel_user_project
- Open MPW Precheck: https://github.com/efabless/open_mpw_precheck

FAQ: https://efabless.com/open_mpw_faq

一生一芯 Initiative

Start From Scratch
Create Your Own
RISC-V® Processor

Everyone is welcome, with no limitation

on

- University
- Major
- Grade level
- Background

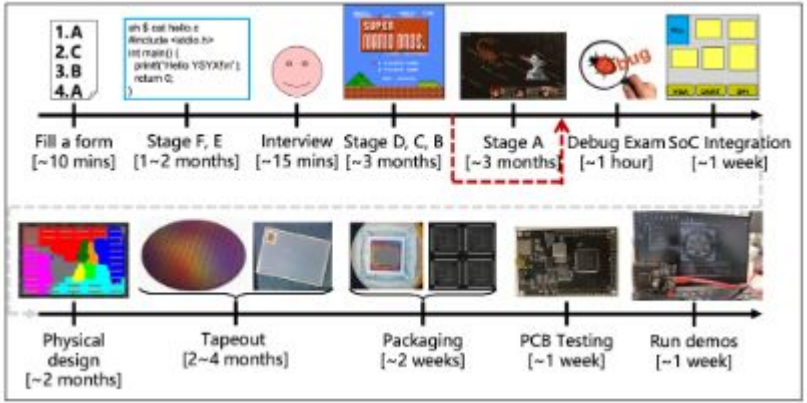
Education equality

- Application
- Runtime
- (Simple) OS
- ISA(RISC-V)
- Micro-architecture
- Circuit
- Synthesis
- Physical design
- Physical verification
- Layout(GDSII)

Full-stack training

Visit https://ysyx.org/en/
Enroll Anytime, Open Year-Round

- **4 years** since inception
- **800 schools** have been involved
- **10,000 students** have participated
- **100 students** have successfully taped out



Students learn to design their own RISC-V processors (RTL->GDSII) using OpenPDK (IHP or SkyWater)

A Massive Open Learning-by-doing Initiative https://ysyx.org/en/

OpenSUSI (Open Source Utilized Silicon Initiative)

CHIPS ALLIANCE

efabless.com

Google

Community

ISHI NSW

東芝情報システム株式会社

一般社団法人 組込みシステム技術協会 Japan Embedded Systems Technology Association

公益財団法人 九州経済調査協会 KYUSHU ECONOMIC RESEARCH CENTER

OPENSUSI

Domestic Foundry

AIST

経済産業省 Ministry of Economy, Trade and Industry

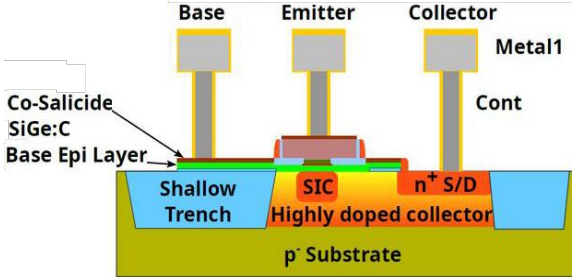
AIST SOLUTIONS

[REF] April 2024, AIST Solutions established the General Incorporated Association OpenSUSI

IHP OpenPDK for SiGe-HBT SG13G2

	SG13S	SG13G2	SG13G3Cu
SiGe-HBT f_t / f_{max}	250 / 340 GHz	350 / 450 GHz	**470 / 650 GHz**
$W_{Emitter}$	170 nm	130 nm	110 nm
HBT BV_{CE0}	1.7 V	1.6 V	1.5 V
CMOS node	**130 nm**		
Active devices	Schottky diodes, Antenna diodes, PN diodes, ESD		
Varactors	NMOS Varactor		
Resistors	Poly-Si, Thin Film		Poly-Si
MIM Caps	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	1.5 fF / µm² (Al) 2.1 fF / µm² (Cu)	2.1 fF / µm²
Metallization	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm)	7 Layers AL incl. 2 & 3 µm layers or *Cu: 4 + 2 (3µm) Al: 2 (3µm	*Cu: 4 + 2 (3µm) Al: 2 (3µm

- Targets are high-end applications for RF & THz frequencies, cryo, space
- SG13G2 is qualified and ready for Low Volume of high-end products it was selected for the development of an open PDK
- SG13G3Cu is early access - qualification scheduled 2025

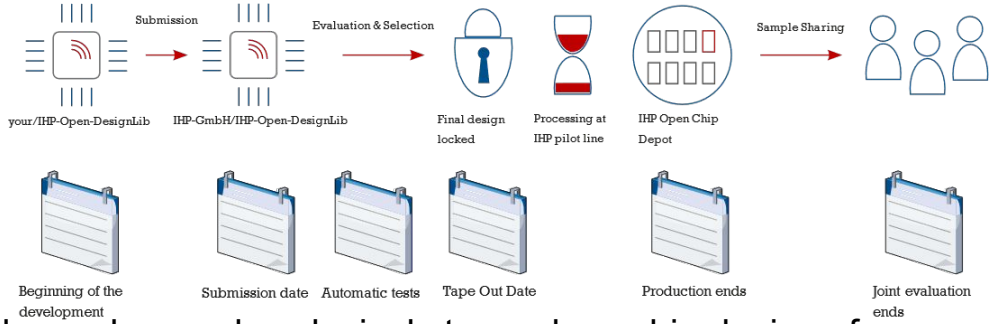


[REF] 130nm BiCMOS **OpenPDK**, dedicated for Analog/Digital, Mixed Signal and RF Design
https://github.com/IHP-GmbH/IHP-Open-PDK
https://github.com/IHP-GmbH/IHP-Open-PDK/wiki/Networking-Workshop-FMD-QNC
https://www.mos-ak.org/bruges_2024/publication/1_Scholz_ESSERC_2024_IHP_OpenPDK.pdf

OpenPDK Support for Open Source IC designs

Schedule of **FREE** MPW Runs in 2025

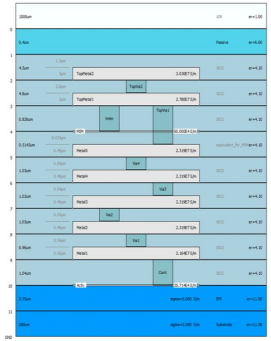
Tape In date	01 Mar 2025	09 May 2025	18 Jul 2025	15 Sep 2025
Technology	SG13G2	SG13G2	SG13G2	**SG13CMOS**
Area available [mm2]	140	30	30	220



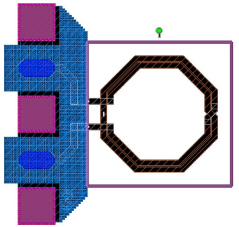
- Project funds can be used exclusively to produce chip designs for non-economic activities, such as university education, research projects, and others R&D institutions
- New procedures to provide free or low-cost MPW area for the open-source community is available, now, all beyond 2026 is under the developments

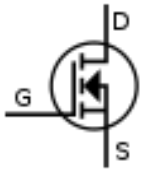
REF: https://ihp-open-ip.readthedocs.io/en/latest/#

OpenPDK Device/Cell Abstract Views

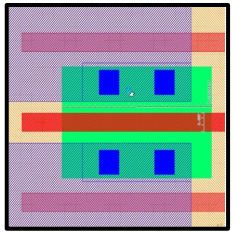


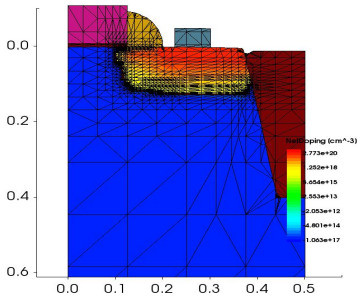

```
# Inductor 3D Numerical Instance
gds_filename = "L_2n0.gds"
XML_filename = "SG13.xml"
script_path = utilities.get_script_path(__file__)
```



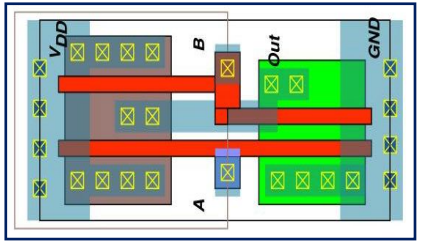



```
* SPICE instance NMOS Card
N1 (d g s b) nmos <i_par=value>
* Model Card
.model nmos psp <m_par=value>
```





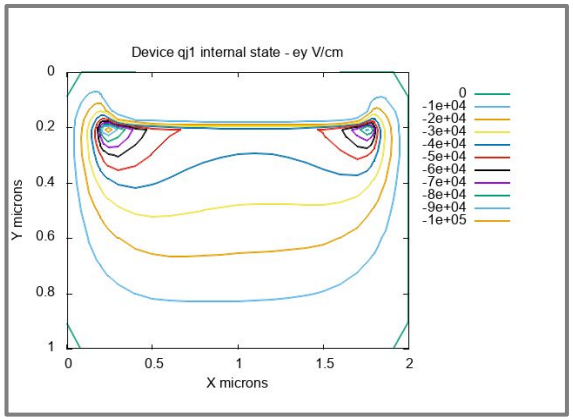
```
// Verilog Instantiate: CMOS NAND gate
//
cmos_nand NAND1 (.a(A), .b(B), .out(Out));
```



Process/TCAD IC Schematic Symbols Numerical/SPICE/Verilog-A Simulations GDSII Layout

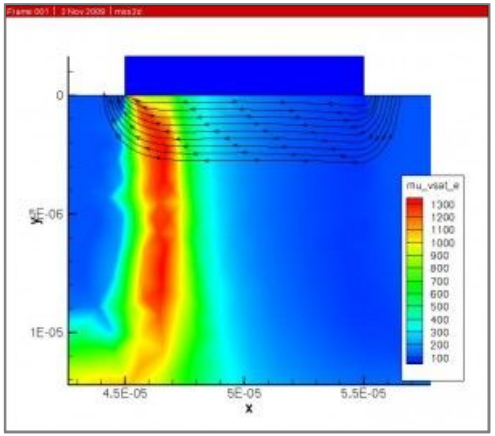
Process TCAD Simulations

- Cider in ngspice



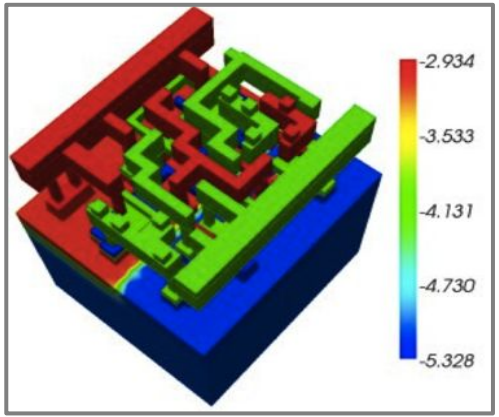
https://sourceforge.net/projects/ngspice/files/

- DevSim TCAD



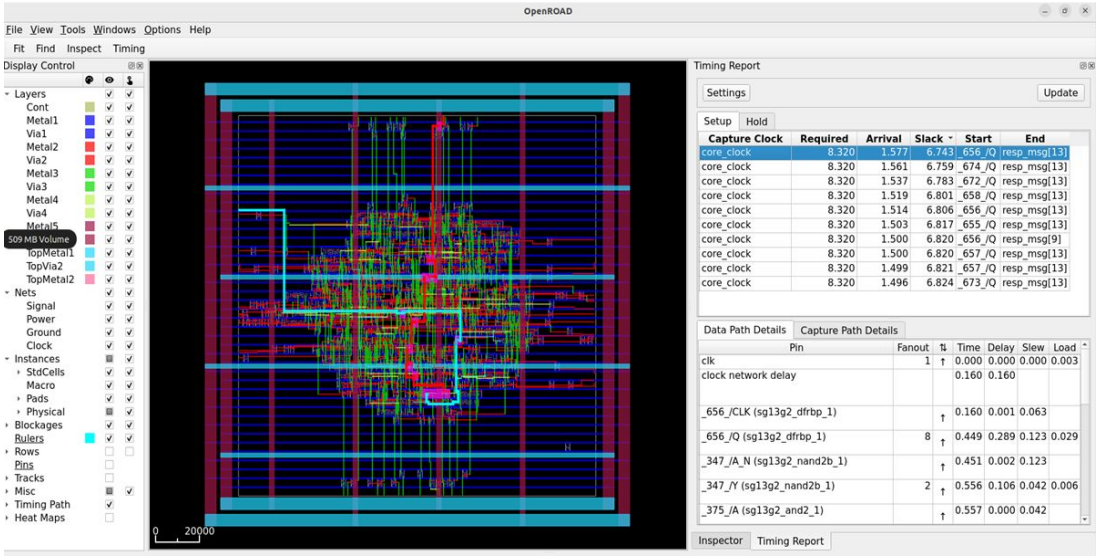
2D MOSFET simulation
https://devsim.org/

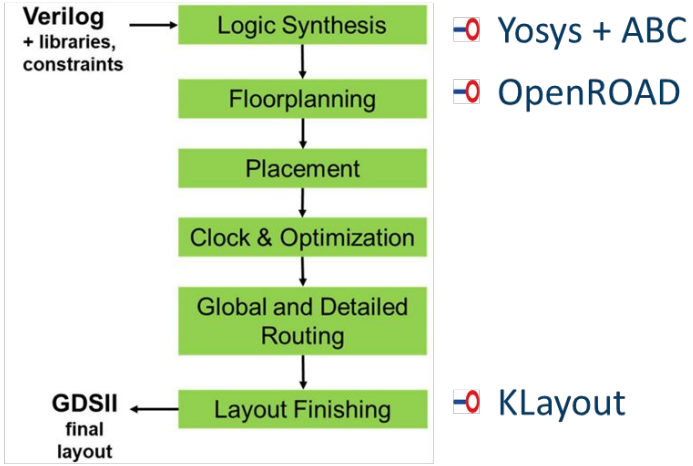
- Cogenda TCAD



3D SRAM Cell
https://cogenda.com/

Open Source Digital Design Flow

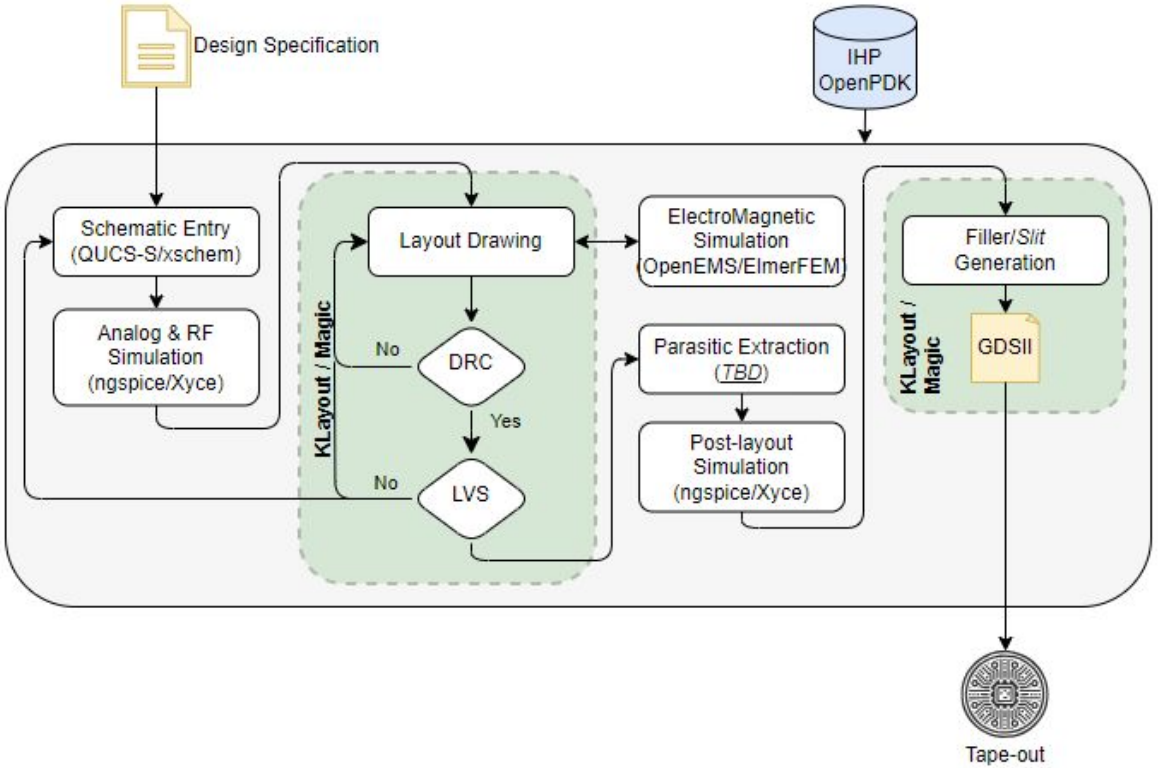




OpenROAD is an open-source EDA tool that automates the entire digital circuit design process from RTL to GDSII, enabling no-human-in-the-loop chip fabrication. Developed under the DARPA IDEA initiative, it aims to democratize access to advanced semiconductor design by providing a free, end-to-end platform for researchers, startups and academia to innovate without proprietary tooling barriers.

[REF] OpenROAD flow scripts:
https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts
Alternative: LiP6 FOSS Logiciels: Alliance, Coriolis, Oceane, Standard Cell Libraries, Tas/Yagle
https://largo.lip6.fr/equipe-cian/logiciels/

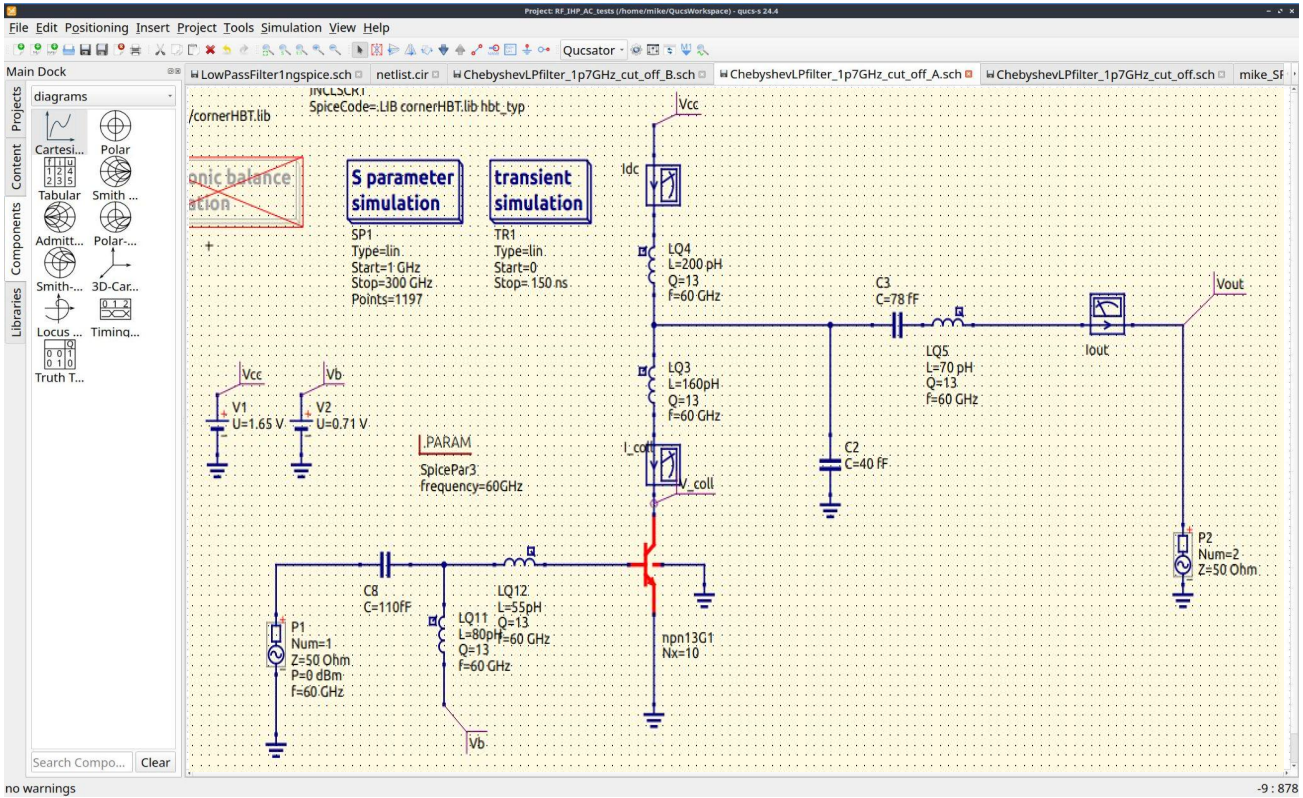
Open Source Analog/RF Design Flow



- QUCS-S, xschem
  - ngspice, xyce
- KLayout, Magic
  - Layout design
  - Parametric cells
  - Physical Verification
- KLayout-PEX tool
- OpenEMS
- other (EMS ElmerFEM)

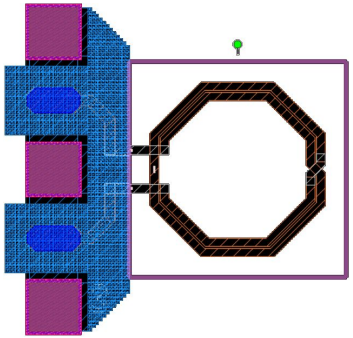
[REF] FOSS EDA Tools Wiki <https://semiwiki.com/wikis/industry-wikis/eda-open-source-tools-wiki/>
IIC-OSIC-TOOLS is an all-in-one Dockers for analog and digital chip design<https://github.com/iic-jku/iic-osic-tools>

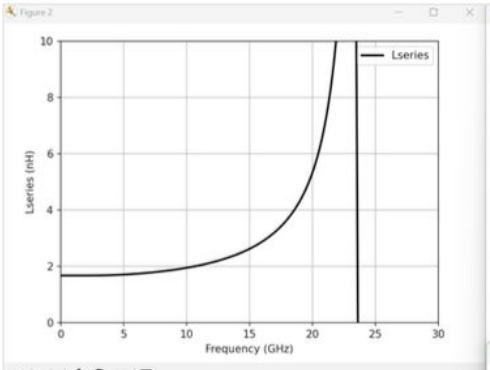
QUCS-S/ngspice Open PDK Custom Lib

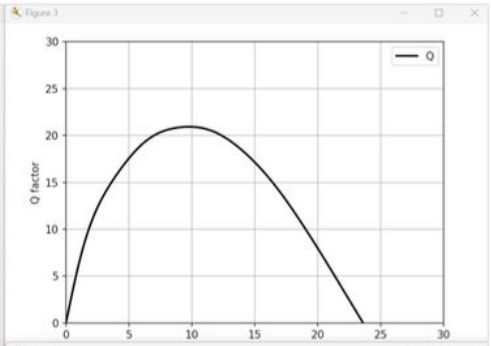


[REF] Qucs-S (ngspice, Xyce) with Qt-based GUI
https://ra3xdh.github.io/

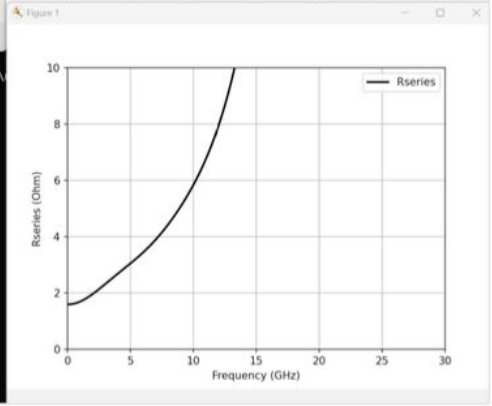
Analog/RF modeling with openEMS








```
7\RUN_MODEL_L2n0.py
Simulation data directory:  p:\ihp\projekte\opdk_2024\openems_2024\
Reading XML stackup  file: SG13.xml
Reading GDSII input file: L_2n0_simplified.gds

-------------------------
Mesh cells by axis (total 1192 kcells):
 x = 177
 y = 153
 z = 44
Smallest cell size:
 dx = 1.2400
 dy = 1.2400
 dz = 0.9600
-------------------------

Frequency [GHz]: 10.05
Series L  [nH] : 1.9492714383268774
Series R  [Ohm]: 5.8806456421489 44
Q factor       : 20.93115718635151
-------------------
L_DC      [nH] : 1.6698471604532308
R_DC      [Ohm]: 1.5909143188844571
Peak Q         : 20.93974772372503
```



[REF] REF: Mustafa Alchalabi and Jan Taro Svejda
“openEMS as a versatile tool in the framework of mm-wave openPDK-based RF chip design”
https://www.mos-ak.org/bruges_2024/publication/5_Svejda_ESSERC_2024_openEMS.pdf
Volker Mühlhaus; Using OpenEMS with IHP SG13 (Python Interface) ver.2.0 December 2024

Compact/SPICE modeling in Verilog-A

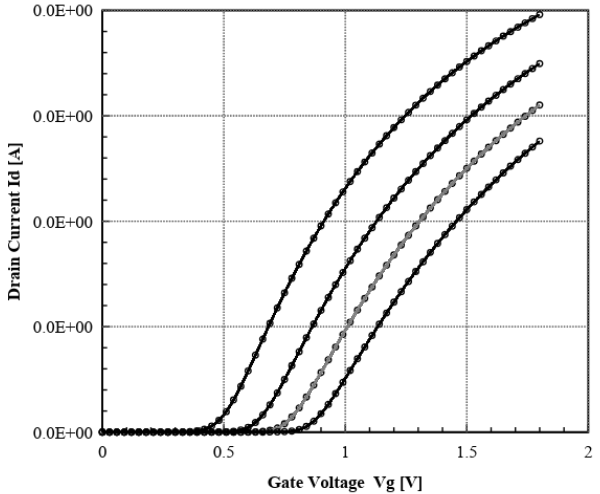
```
`include "std.va"
`include "const.va"
// ***********************************
// * EKV MOS model (long channel)
// * https://ekv.epfl.ch/Verilog-A/
// ***********************************
module ekv(d,g,s,b);
        //
        // Node definitions
        inout d,g,s,b ; // external nodes
        electrical d,g,s,b ; // external nodes
        //
        //*** Local variables
        real x, VG, VS, VD, VGprime, VP;
        real beta, n, iff, ir, Ispec, Id;
        //
        //*** model parameter definitions
        parameter real L = 10E-6 from[0.0:inf];
        parameter real W = 10E-6 from[0.0:inf];
        //*** Threshold voltage
        // substrate effect parameters (long-channel)
        parameter real VTO = 0.5 from[0.0:inf];
        parameter real GAMMA = 0.7 from[0.0:inf];
        parameter real PHI = 0.5 from[0.2:inf];
        //*** Mobility parameters (long-channel)
        parameter real KP = 20E-6 from[0.0:inf];
        parameter real THETA = 50.0E-3 from[0.0:inf];
```

```
analog begin // EKV v2.6 long-channel
        VG = V(g); VS = V(s); VD = V(d);
        // Effective gate voltage (33)
        VGprime = VG - VTO + PHI + GAMMA * sqrt(PHI);
        // Pinch-off voltage (34)
        VP = VGprime - PHI - GAMMA
        * (sqrt(VGprime+(GAMMA/2.0)*(GAMMA/2.0))-(GAMMA/2.0));
        // Slope factor (39)
        n = 1.0 + GAMMA / (2.0*sqrt(PHI + VP + 4.0*$vt));
        // Mobility equation (58), (64)
        beta = KP * (W/L) * (1.0/(1.0 + THETA * VP));
        // forward (44) and reverse (56) currents
        x=(VP-VS)/$vt;
        iff = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
        x=(VP-VD)/$vt;
        ir = (ln(1.0+exp(x/2.0)))*(ln(1.0+exp(x/2.0)));
        // Specific current (65)
        Ispec = 2 * n * beta * $vt * $vt;
        // Drain current (66)
        Id = Ispec * (iff - ir);
        //
        // Branch contributions to EKV v2.6 model (long-channel)
        //
        I(d,s) <+ Id;
end // analog
endmodule
```

EKV2.6 Compact MOSFET Model Standard for Analog/RF IC Designs
https://github.com/ekv26/model
EKV3 MOSFET model in Verilog-A
https://github.com/MatBucher/ekv3model/
Alternative: ACM2 (Advanced Compact MOSFET) charge-based physical model
https://github.com/ACMmodel/MOSFET_model/tree/main/Examples/IHP-SG13

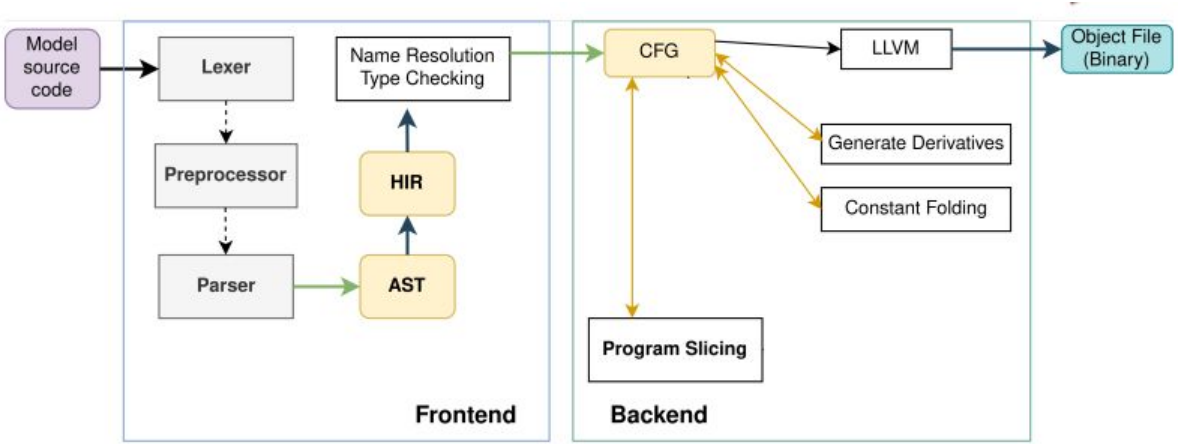
Compact/SPICE modeling in Verilog-A

```
* EKV long channel MOSFET Model

.osdi  ekv.va

vd  1  0 0.05
vg  2  0 2
vs  3  0 0
vb  4  0 0

xekv  1 2 3 4 ekv L=1E-6 W=1E-6

.dc vg 0 2 0.1

.end
```



NLnet - "Test Procedures for MOSFET Open Source SPICE Model Validation"
The aims to establish such tests for the compact models in open PDKs, which are intended to be generic enough for model quality assurance testing with FOSS circuit simulators such as GnuCAP, ngspice, xyce, Qucs-S, among others.
https://nlnet.nl/project/MOSFET-testprocedures/

OpenVAF: Next-Generation Verilog-A compiler

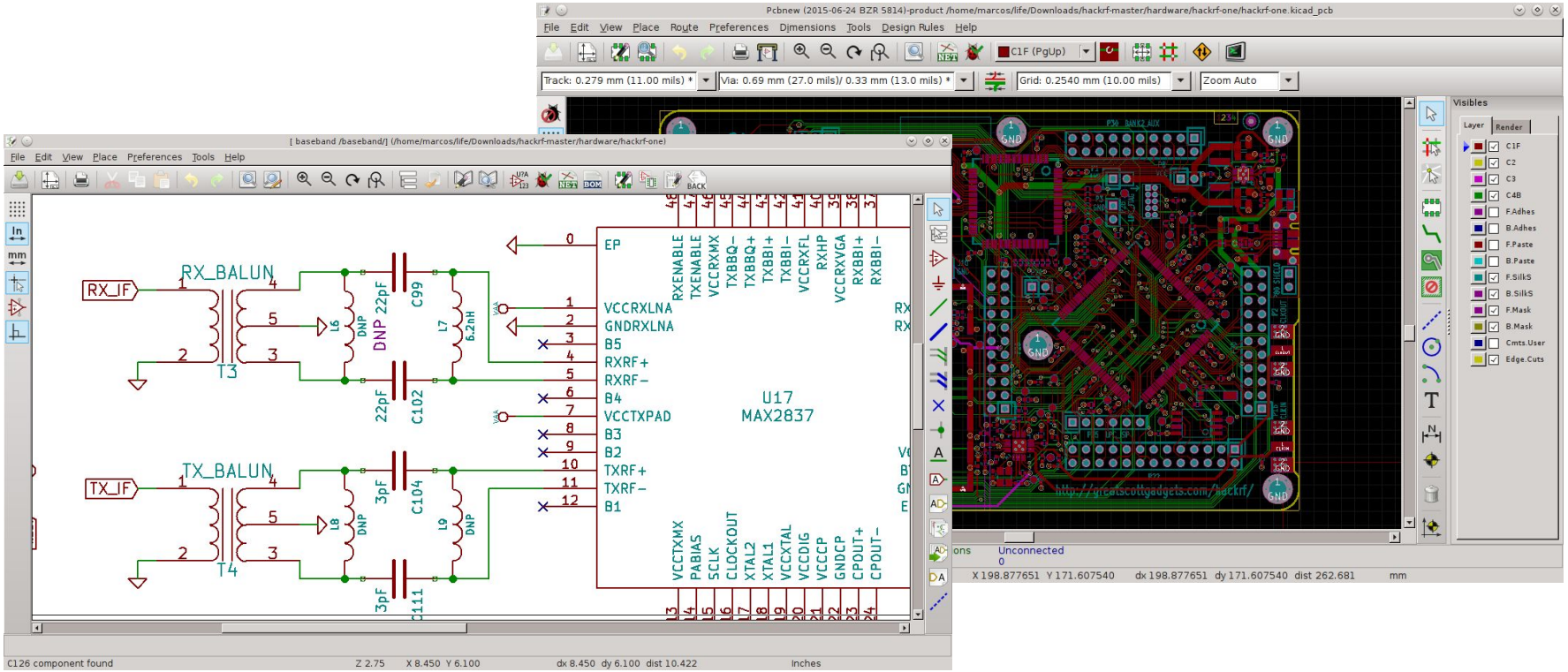


OpenVAF Roadmap

- Reaching full compliance with the Verilog-A standard on OpenPDK
- OSDI integration in ngspice and Xyce
- Noise analysis (released with ngspice-42*)
- Improved documentation

[REF] P. Kuthe, M. Muller; OpenVAF is a Next-Generation Verilog-A compiler
<https://openvaf.semimod.de/>
Árpád Bűrmen; VACASK and Verilog-A Distiller
<https://fosdem.org/2025/schedule/event/fosdem-2025-4681-vacask-and-verilog-a-distiller-building-a-device-library-for-an-analog-circuit-simulator/>
Alternative: Felix Salfelder and Al Davis; Verilog-AMS in Gnucap
<https://fosdem.org/2025/schedule/event/fosdem-2025-5880-verilog-ams-in-gnucap/

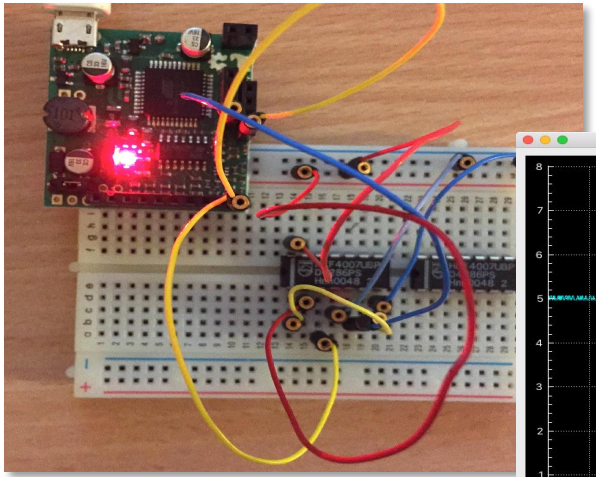
ngspice and KiCAD



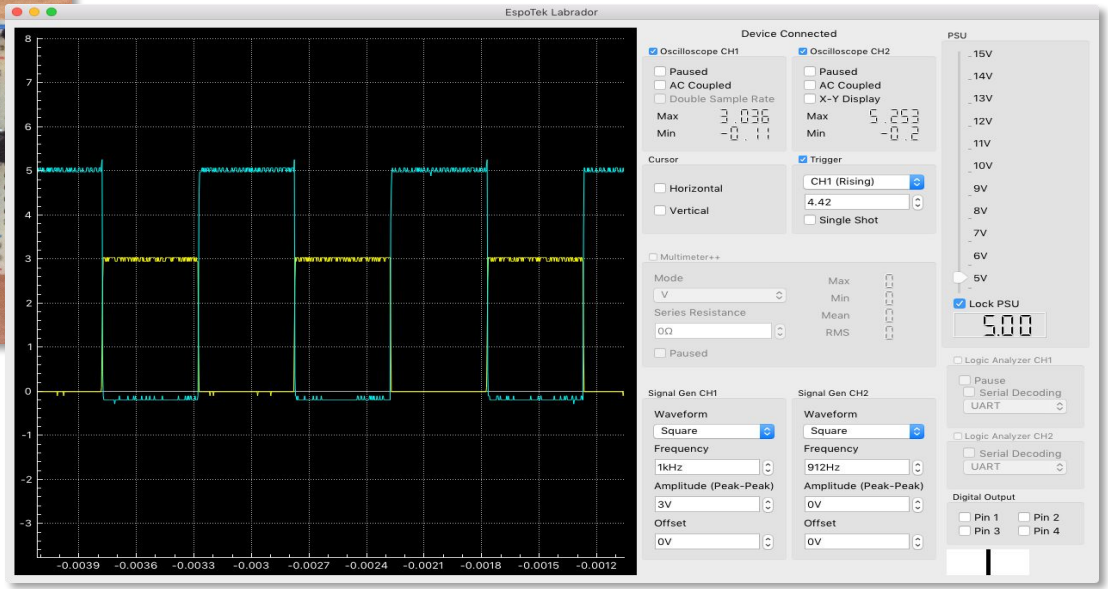
[REF] https://www.kicad.org/download/

Holger Vogt; ngspice - XSPICE elemental devices made available in KiCad
https://fosdem.org/2025/schedule/event/
fosdem-2025-5619-ngspice-xspice-elemental-devices-made-available-in-kicad/

EspoTek Labrador Circuit Lab



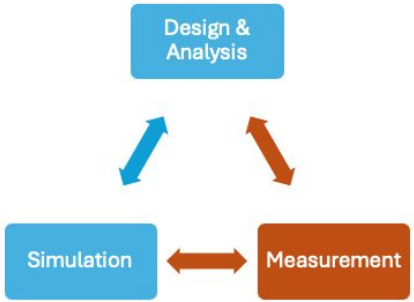
4007 CMOS inverter chip measurement

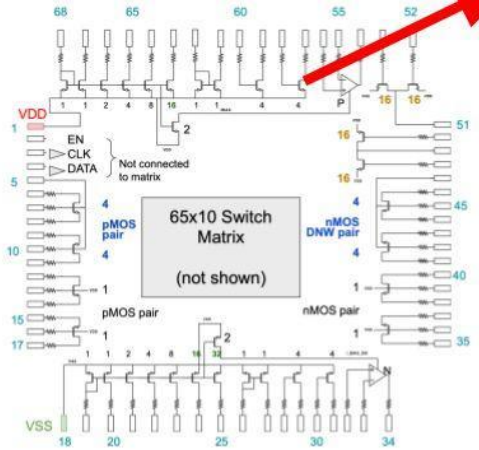


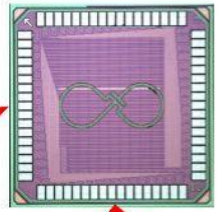
[REF] https://espotek.com/labrador

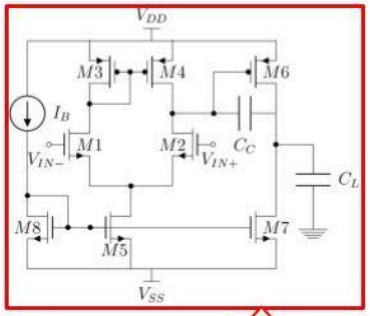
https://archive.fosdem.org/2018/schedule/event/cad_spice/

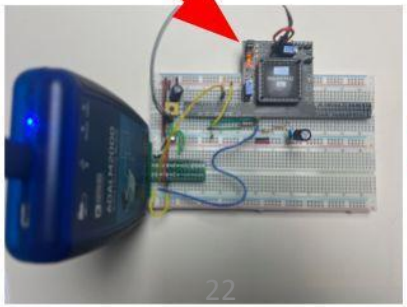
MOSbius: Chip to Support CMOS Circuit Labs







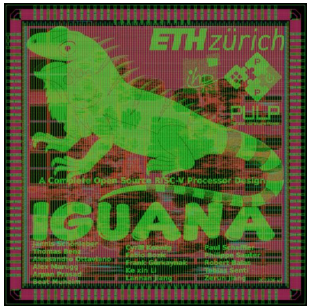




- Teaching students the **connection between design/simulation and measurements**
  - https://mosbius.org
  - https://www.linkedin.com/posts/peter-kinget-7481a3_want-to-offer-your-students-hands-on-labs-activity-7274878090617524225-iGPm
- Great tool for workforce development by Prof. Peter Kinget at Columbia University

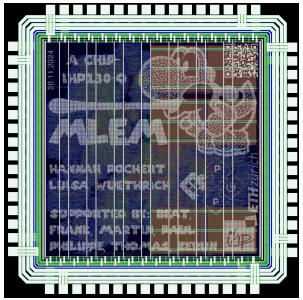
Columbia Integrated Systems Laboratory
http://www.cisl.columbia.edu

Digital Designs in IHP OpenPDK

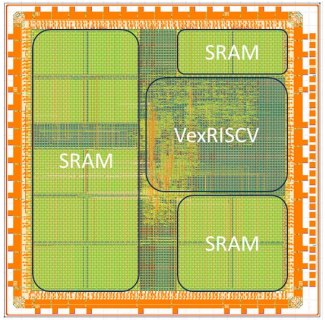


Iguana: http://asic.ethz.ch/2023/Iguana.html

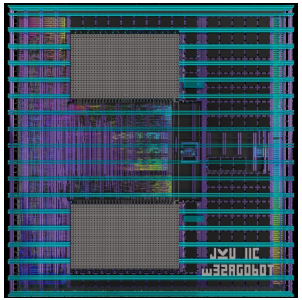
Basilisk: http://asic.ethz.ch/2024/Basilisk.html



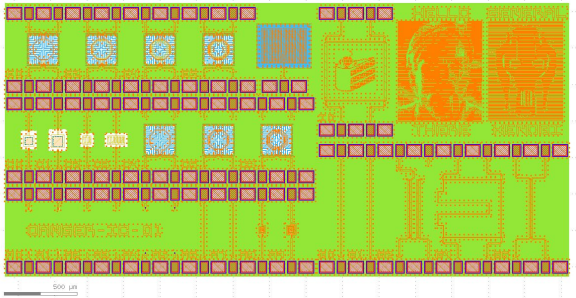
Mlem: http://asic.ethz.ch/2024/MLEM.html



https://github.com/HEP-Alliance
IHP Open Hardware Security Module

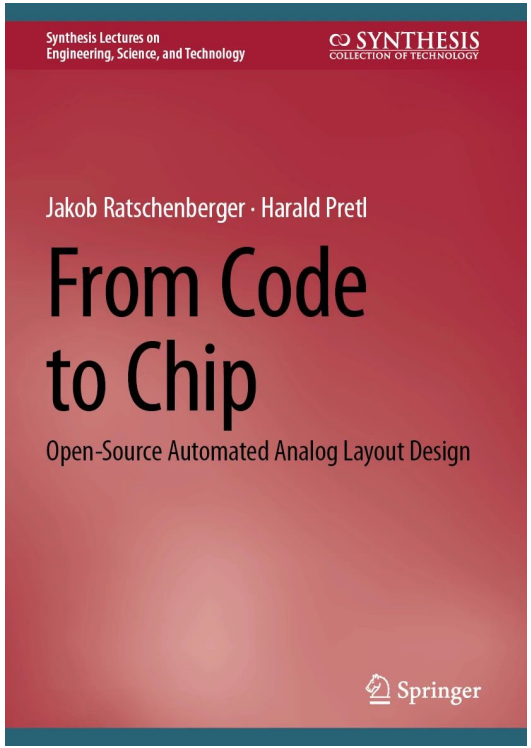


https://github.com/iic-jku/SKY130_SAR-ADC1
to be ported into IHP OpenPDK



Open source analog/RF IC by JKU Linz
https://gdsfactory.github.io/gdsfactory/

From Code to Chip



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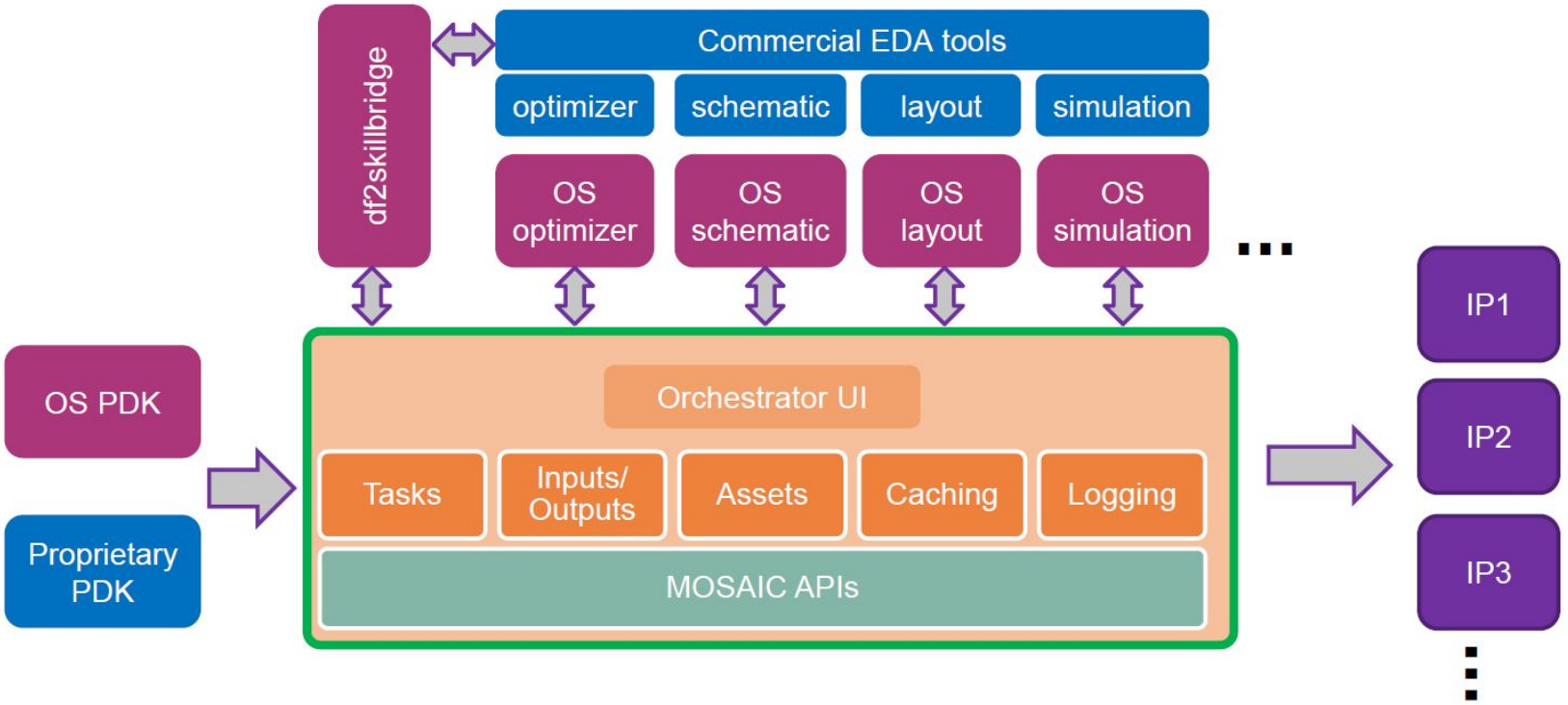
- Experimental Results pp. 73-99
- Outlook pp. 101-103
- Back Matter pp. 105-120

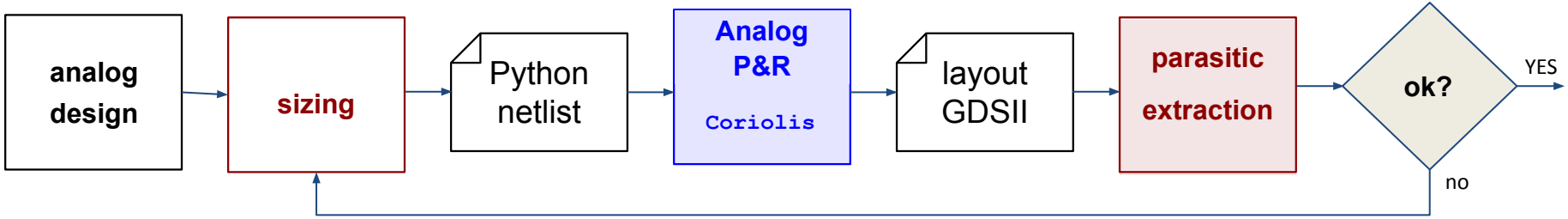
[book] Jakob Ratschenberger and Harald Pretl; From Code to Chip: Open-Source Automated Analog Layout Design; pp: XV, 120 Publisher: Springer (2025) eBook ISBN 978-3-031-68562-0

MOSAIC: Modular Framework



REF: https://www.mos-ak.org/bruges_2024/publication/6_Sandner_ESSERC_2024_openIC.pdf
https://www.mosaic-ic.org/

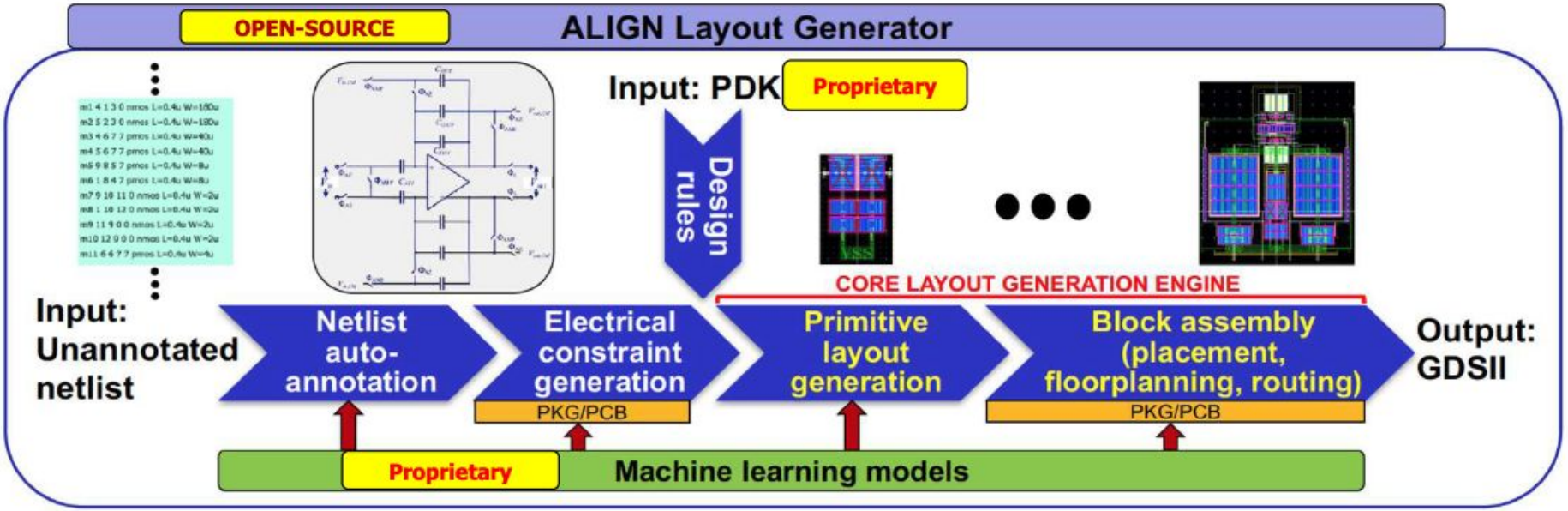
CORIOLIS – Analog Capabilities



- CORIOLIS focus on the P&R stage. Makes the assumption that the parasitics extraction do not fundamentally change the topological characteristics of the design. That is only slight size adjustment of the components may be needed, so the overall topology remains valid.
- [REF] Jean-Paul CHAPUT, CIAN Team, <Jean-Paul.Chaput@lip6.fr>

LIP6 SCIENCES SORBONNE UNIVERSITÉ cnrs

ALIGN: Layout generation netlist > GDSII



[REF] Sachin S. Sapatnekar, University of Minnesota, ALIGN-analoglayout
Open-source software at https://github.com/ALIGN-analoglayout/ALIGN-public
https://www.mos-ak.org/silicon_valley_2021/presentations/Sapatnekar_MOS_AK_SV_2021.pdf

What's next?
FOSS to Empower Researchers and IC Designers

FOSS eSim offers similar capabilities and ease of use as any equivalent proprietary software for schematic creation, simulation and PCB design, without having to pay a huge amount of money to procure licenses [REF] https://esim.fossee.in/

The **SSCS PICO Program**: Democratizing IC Design; first open-source IC design contest. Silicon fabrication using **open** SKY130, GF180MCU PDK on eFabless' chipIgnite shuttle
[REF]https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program

The Universalization of IC Design from CASS (**UNIC-CASS**) program is a structured end-to-end Integrated Circuit (IC) design-to-test experiential learning
[REF] https://ieee-cas.org/universalization-ic-design-cass-unic-cass

RISC-V is a **free and open** ISA enabling for a new era of processor innovation through open collaboration. Offers a new level of free, extensible software and hardware freedom on architecture, paving the way for the years ahead of computing design and innovation
[REF https://riscv.org/about/

Open-Source EDA Roadmap for Europe

A first version of the roadmap and recommendations was presented at ORConf 2024 (with the recording). In the community review period after this, we have received and incorporated over 70 individual contributions. This document describes the opportunities provided by open-source tools for chip design and how funding work on them could contribute to the goals of the European Commission. It provides recommendations for funding opportunities that close gaps in the important OpenPDK and FOSS CAD/EDA focus areas.
Three short-term actions have been identified to foster the roadmap:

- Open Source Analogue and Mixed-Signal Designs for Europe
- Productivity, Interoperability and Verification for more European Chips
- System-on-Chip Innovation from Europe with Open-Source Digital Chip Design

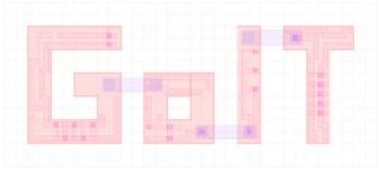
Version: November 19, 2024 - Public Release
<https://tinyurl.com/OpenSourceEDARoadmap>

Acknowledgment

René Scholz, Sergei Andreev, Krzysztof Herman, Alexey Balashov, Mario Krattenmacher, Pascal Kuthe, Markus Müller, Jean-Michel Sallese, Matthias Bucher, Daniel Tomaszewski, Guilherme Torri, Bal Virdee, Mike Brinson, Matthias Köfferlein, Thorsten Liebig, Jan Taro Svejda, Al Davis, Felix Salfelder, Francesco Lannutti, Paolo Nenzi, Dietmar Warning, Holger Vogt, Volker Mühlhaus, Murat Eskiyerli, Eric Keiter, Jason Verley, Yungang Bao, Luca Benini, Frank Gurkaynak, Luca Alloatti, Thomas Kramer, Marie-Minerve Louerat, Jean-Paul Chaput, Kannan Moudgalya, Sumanto Kar, Harald Pretl, Boris Murmann, Mehdi Saligane, Peter Kinget, Matt Venn, Tim Ansell

- The IHP OpenPDK Team with Sergei Andreev, Project Lead
- ETH Zurich + JKU Linz + IIT Bombay, all the open source community
- German public funded projects:
  - VE-HEP (16KIS1339K) https://elektronikforschung.de/projekte/ve-hep-1
  - IHP Open130-G2 (16ME0852) https://www.elektronikforschung.de/projekte/ihp-open130-g2
  - FMD-QNC (16ME0831) https://www.elektronikforschung.de/projekte/fmd-qnc
  - FMD-QNC with VDI/VDE (IHP PDK Workshop funding)

Open-Source EDA Roadmap Acknowledgment



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- Olof Kindgren; Qamcom
- Thomas Parry; SPHERICAL
- Harald Pretl; Johannes Kepler University, Linz
- Tomi Rantakari; ChipFlow
- Rene Scholz; IHP OpenPDK
- Matthew Venn; YosysHQ, Tiny Tapeout and FOSSi Foundation
- Mirjana Videnovic-Misic; Infineon Technologies
- Stefan Wallentowitz; Hochschule München and FOSSi Foundation

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Version: November 19, 2024 - Public Release
<https://tinyurl.com/OpenSourceEDARoadmap>

MOS-AK: 2025 Events

- OpenPDK at FOSDEM, Bruxelles (B) Feb. 1-2, 2025
- OpenPDK at EDTM, Hong Kong, March 9-12, 2025
- OpenPDK at FSiC, Frankfurt (O) July 2-4 2025
- ICMC/DAC'25 San Francisco (US) June 26-27, 2025
- OpenPDK Tutorial at MIXDES, Szczecin (PL) June 26-28, 2025
- MOS-AK Workshop, London (UK) July 2025
- 9th Sino MOS-AK Workshop, China Aug. 2025
- 22st MOS-AK at 51st ESSERC, Munich (D) Sept. 8-11, 2025
- 18th MOS-AK Workshop Silicon Valley, Dec. 2025

contact: wladek@mos-ak.org