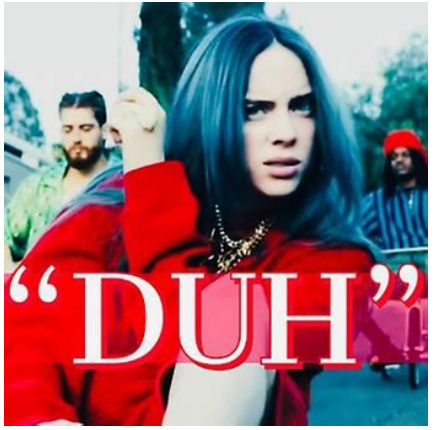
A Love Letter to...

KiCAD ERC

You don’t really love the ERC

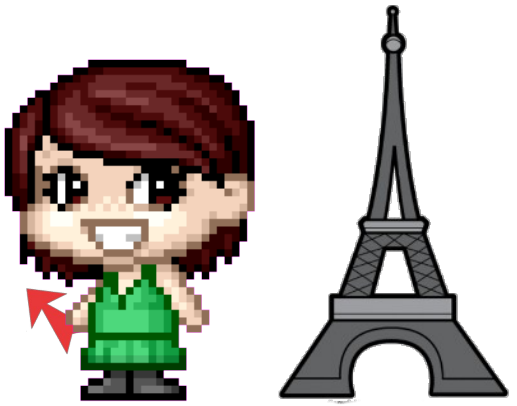
Electrical **R**ules **C**heck

- Reviewed KiCAD designs
  - Found leftover ERC warnings
  - Or unfairly waived ones
- But ERC is so great!
  - Protecting you from potential mistakes
  - Let’s see why, and how!



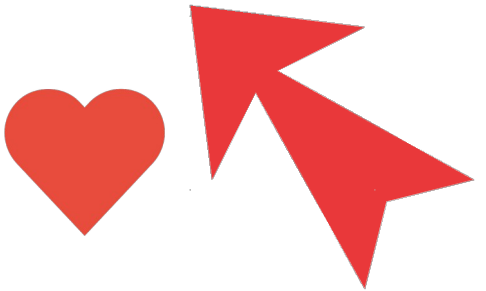
About me

- Eve Redero – redero.fr
- Electronics and embedded engineer
- 10+ years XP in consumer electronics
- ~2 years KiCAD user
  ~5 years Altium
  ~1 year EagleCAD



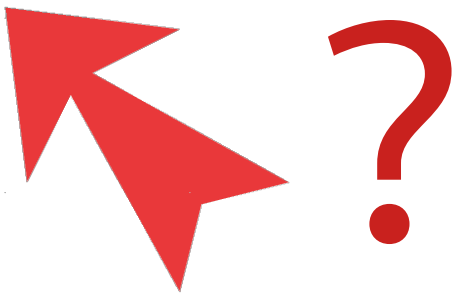
Summary

1. What is ERC?
2. My top 5 ERC
3. How to get rid of this weird ERC message?
4. Pin types and connection matrix
5. ERC vs real life issues (with quizz)



KiCAD is V9

1- What is ERC



Electrical Rules Check

- Set of heuristics related to the schematics and netlist
  - If pin in component not connected, then ERC error
  - If net not connected to anything, then ERC error
- Similar to software warnings

What ERC is not...

- Spice simulators:
  - Solve electrical equations
  - Integration with KiCAD
  - LTSpice is another popular option
- ERC do not run Spice!
  - Or any kind of simulations

U=RI
q=LdI/dt

Why ERC?

« Most of the time, the consequences for ignoring warnings are nothing, no big deal. However, many of the hard faults […] could have been found by enabling all compiler warnings and fixing each one.
Spend time removing the seemingly trivial compiler warnings so you can see the incredibly important ones. »

Elecia White, Making Embedded Systems (p261)

→ Same with ERC

3 real-life errors I have made

that could have been avoided with a better ERC usage

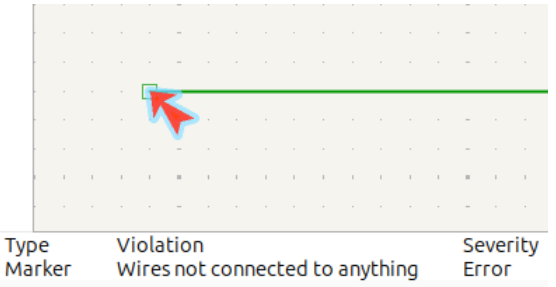
they where manufactured and I had to live with it until the next prototype run

and it cost my company money and time and everyone was mad

1. Power supply not connected because of a typo in net label
   e.g. VDD_3V3 vs VDD-3V3
   → *Microprocessor not powering up*
2. Wrong footprint on a peripheral IC
   → *No peripheral chip equipped, no possible rework*
3. UART TX / RX inverted… twice
   → *No debugging, no flashing*

Run the ERC

- Inspect → Electrical Rules Checker
- Possible to assign key shortcut
- Tip : ERC markers
  - Can be moved or deleted
  - Appear in the status bar

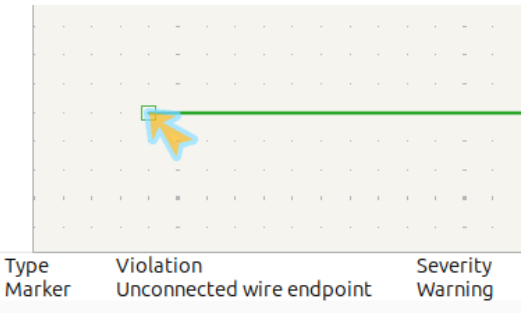


- Run with command line (and in CI!)
  - Kicad-cli (installed with KiCAD)

```
kicad-cli sch erc myfile.kicad_sch –format=json
```

  - Kibot (third-party project)

```
kibot -c .ci/config.kibot.yaml
-e cad/myfile.kicad_sch
```



What is the netlist?

Under the hood, schematics get compiled in a **netlist**

- List of nets and nodes connected to them
- Transmitted to PCB Editor

```
(nets
  (net (code 1) (name GND)
    (node (ref R14) (pin 2))
    (node (ref P4) (pin 2))
    (node (ref C4) (pin 2))
    (node (ref C5) (pin 2))
    (node (ref U2) (pin GND))
    (node (ref U1) (pin 3))
    (node (ref R11) (pin 2))
    (node (ref P5) (pin 2))
    (node (ref C11) (pin 1))
    (node (ref R18) (pin 2))
    (node (ref C7) (pin 2))
    (node (ref C12) (pin 2))
    (node (ref C8) (pin 2))
    (node (ref P6) (pin 2))
    (node (ref Q3) (pin C))
    (node (ref R4) (pin 2))
    (node (ref R8) (pin 2))
    (node (ref P3) (pin 2))
    (node (ref P1) (pin 2))
    (node (ref R21) (pin 2))
    (node (ref C9) (pin 2))
    (node (ref Q7) (pin C))
    (node (ref C2) (pin 2))
    (node (ref P2) (pin 2))
    (node (ref C1) (pin 2))
    (node (ref C14) (pin 2)))
  (net (code 2) (name "Net-(U1-Pad7)")
    (node (ref U1) (pin 7)))
  (net (code 3) (name "Net-(U1-Pad6)")
```

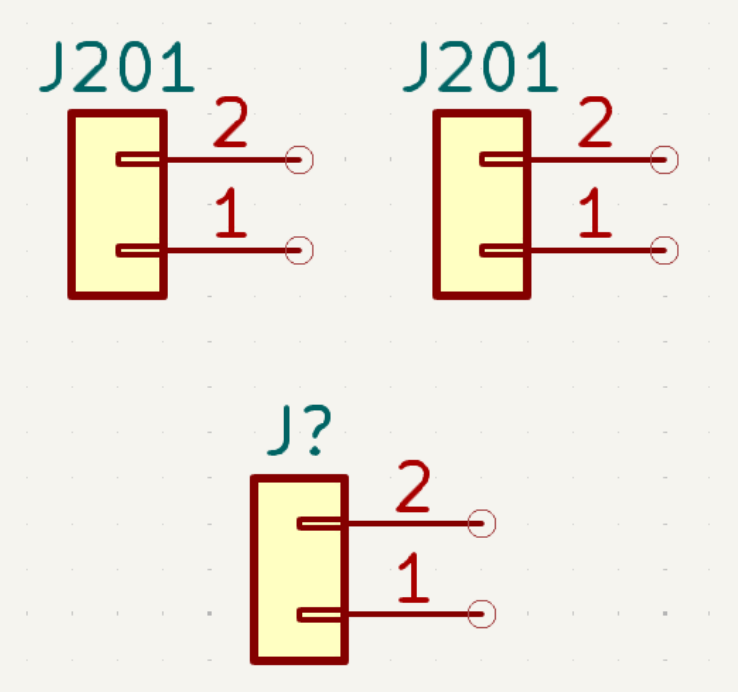
2- My top 5 ERC

Annotations issues

Duplicate items
  - Same annotation used twice

Item not annotated
  - Annotation with « ? »

- Netlist : generated based on symbols annotations
  → Annotation issues are bad
- Tools → Annotate Schematics



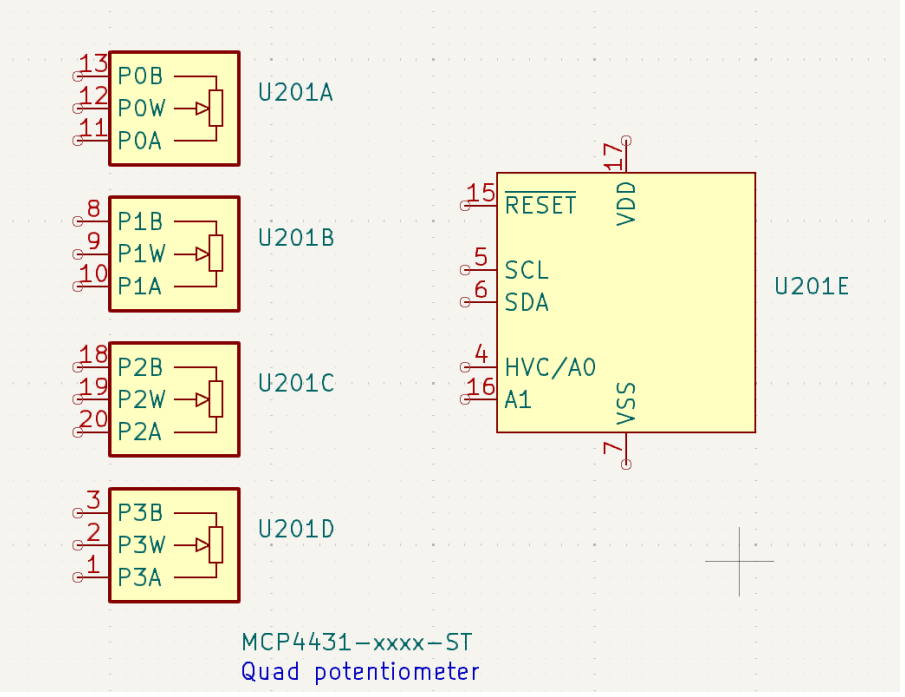
ERCE_UNANNOTATED
ERCE_DUPLICATE_REFERENCE

Missing part in symbols

“Symbols have unplaced units“

Several symbols, one component

- Powerful! Use it!
- Easy to forget one of those symbols
- Potential catastrophe: chip not supplied at all

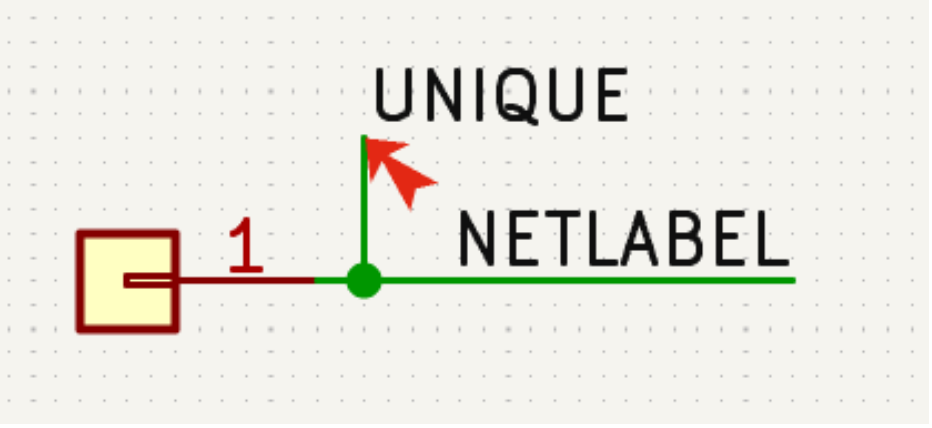


ERCE_MISSING_UNIT

Multiple labels on a net

"Both X and Y are attached to the same items, X will be used in the netlist"

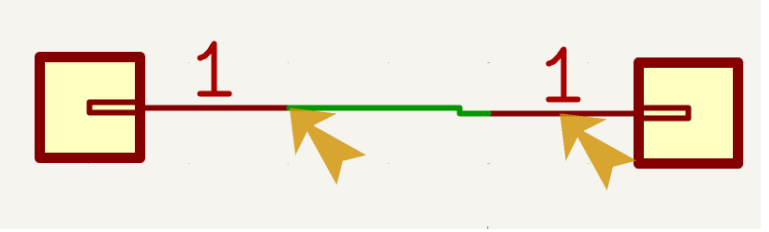
- More than one name given given to this bus or net
- In the netlist, only one net name is chosen
  - Top of the hierarchy if hierarchical
  - Otherwise, IDK
- Annoying because lots of features depend on net names!
  - Differential pair
  - Bus membership

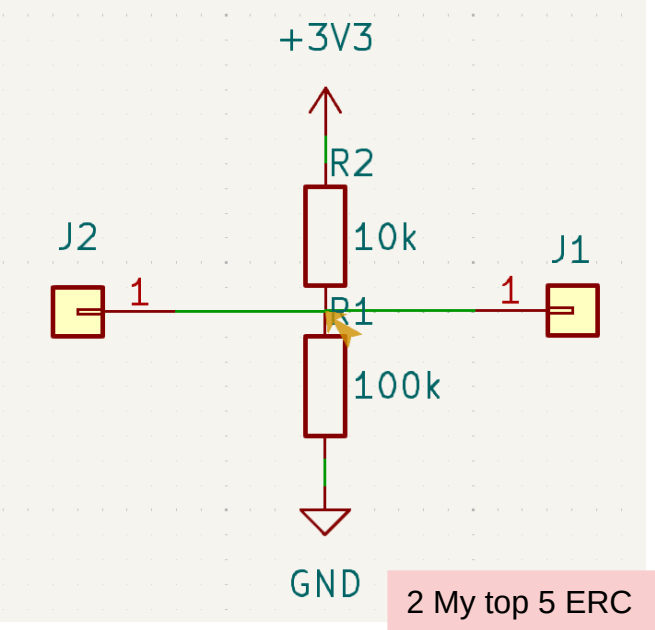


Offgrids

"Symbol pin or wire end off connection grid"

- Offgrid is bad
  - Objects need to be at the exact same coordinates to be connected
  - Off grid things can be close enough to appear connected
- Set up grid correctly
  - 50 or 100 mils
- Use « Align Items to Grid »
- If lib symbol is offgrid, burn the lib





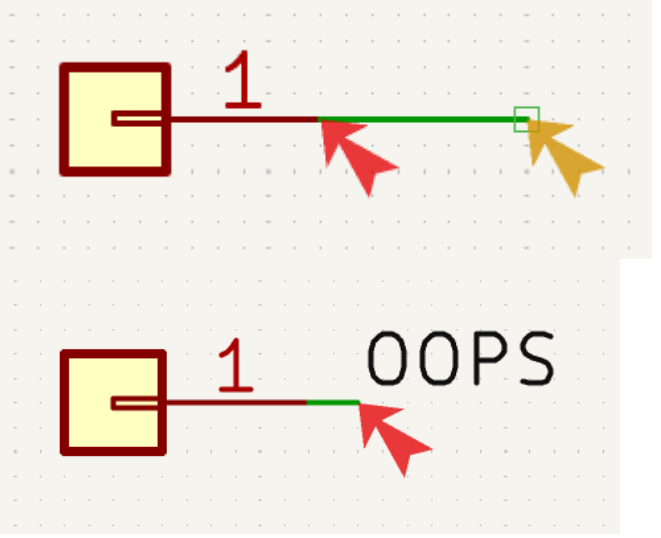
ERCE_ENDPOINT_OFF_GRID

2 My top 5 ERC

Pin / label not connected

- “Pin not connected“
- “Label not connected to anything“

- Object is all alone in the netlist
- Maybe you forgot a really important connection!



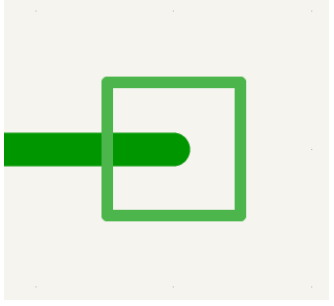

```
(net (code "17") (name "/OOPS") (class "Default")
  (node (ref "J112") (pin "1") (pinfunction "Pin_1") (pintype "passive")))
```

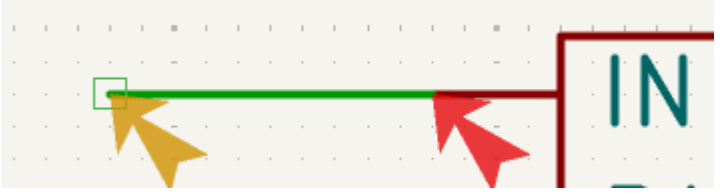

ERCE_PIN_NOT_CONNECTED
ERCE_LABEL_NOT_CONNECTED

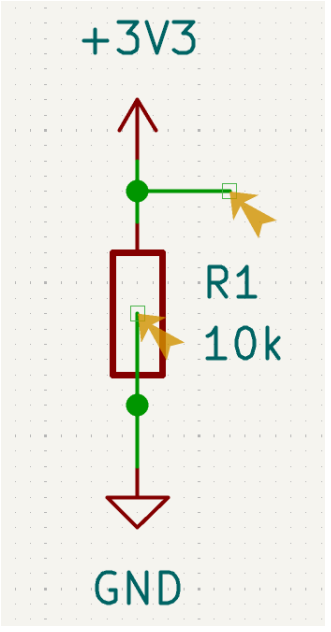
Not connected & loose ends

"Unconnected wire endpoints"

- Graphical only, not compiled
- Good friends with "Not Connected" issues
- Remove them all





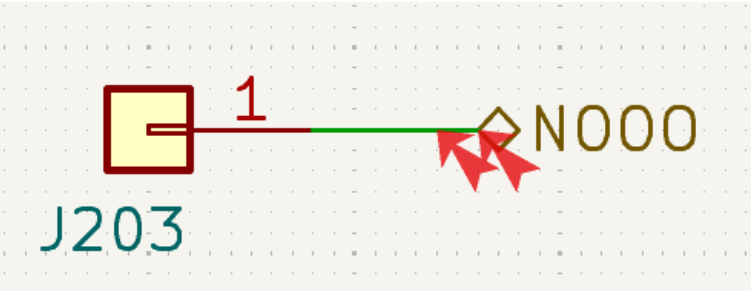


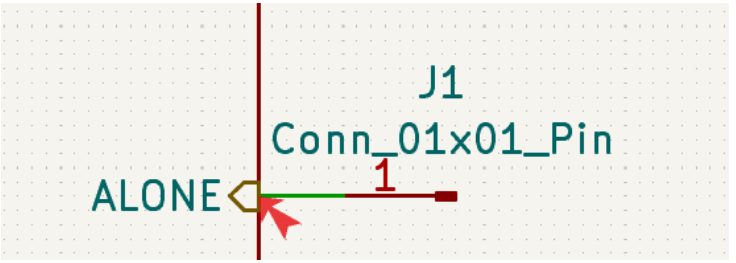
ERCE_UNCONNECTED_WIRE_ENDPOINT

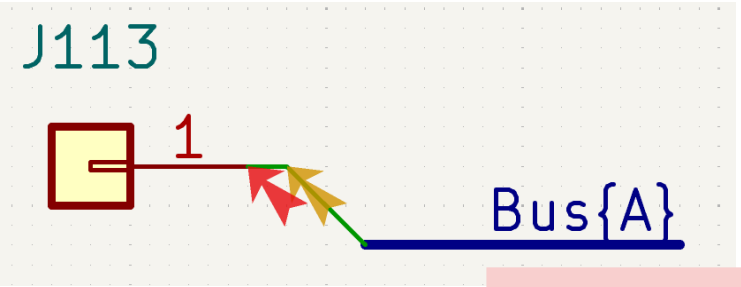
Not connected & fancy errors

Other ways to get a non-connected label:

- “Hierarchical label has no matching sheet pin in the parent sheet“
- “Sheet pin has no matching hierarchical label inside the sheet“
- “Graphically connected to a bus not a member of that bus“



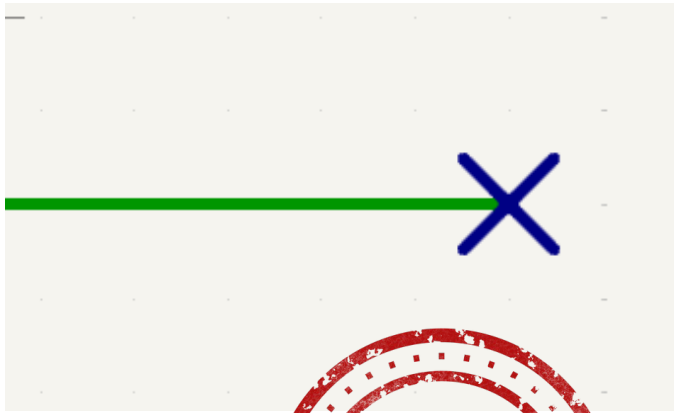




ERCE_HIERACHICAL_LABEL
ERCE_BUS_ENTRY_CONFLICT

2 My top 5 ERC

No connect flag



All pins and nets should be connected...
Unless explicitely exempt by a no-connect flag
- Visual indication
- Stamp of approval

If no-connect flag is connected,
it will raise an ERC too

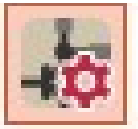
ERCE_NOCONNECT_CONNECTED

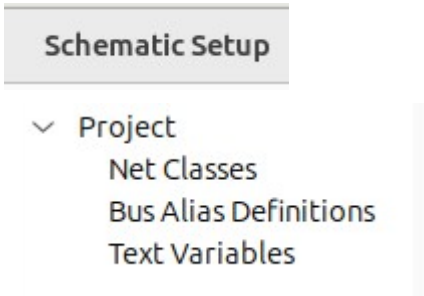
3- How to get rid of weird ERC messages?

Gotta clean them all!

Unresolved variable

- A text with a ${VAR} is written, but no VAR is defined
- Define VAR in the Text Variables submenu
- Not in nets! ${NET} will stay ${NET}

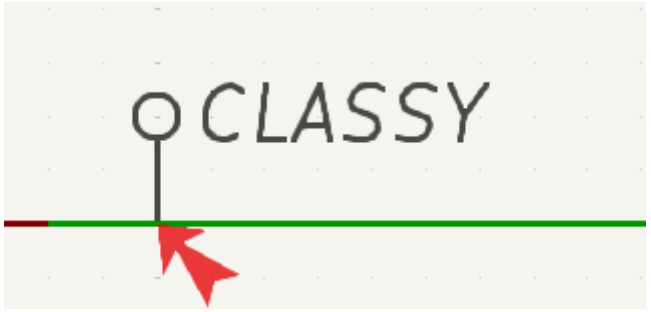


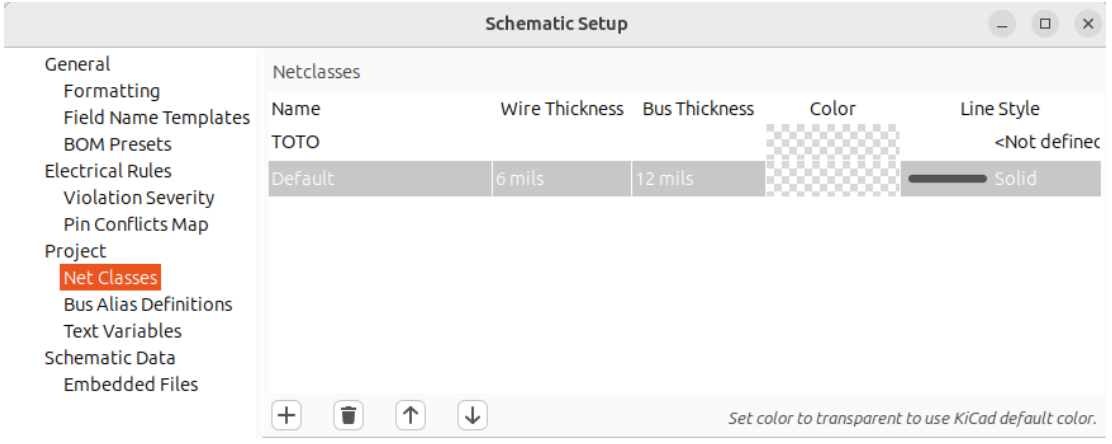


ERCE_UNRESOLVED_VARIABLE

Netclass not defined

- Invoke a netclass with a netclass indicator
- Define the netclass in the Net Classes submenu



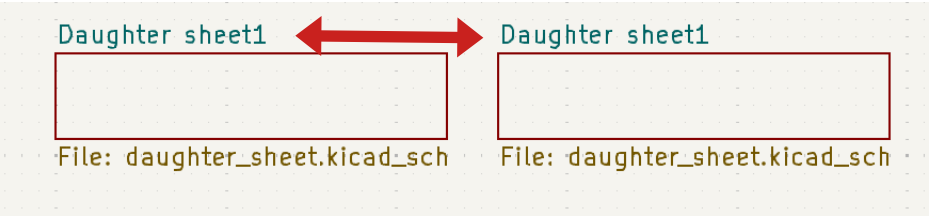


ERCE_UNDEFINED_NETCLASS

Duplicate sheets

"Duplicate sheet names within a given sheet"

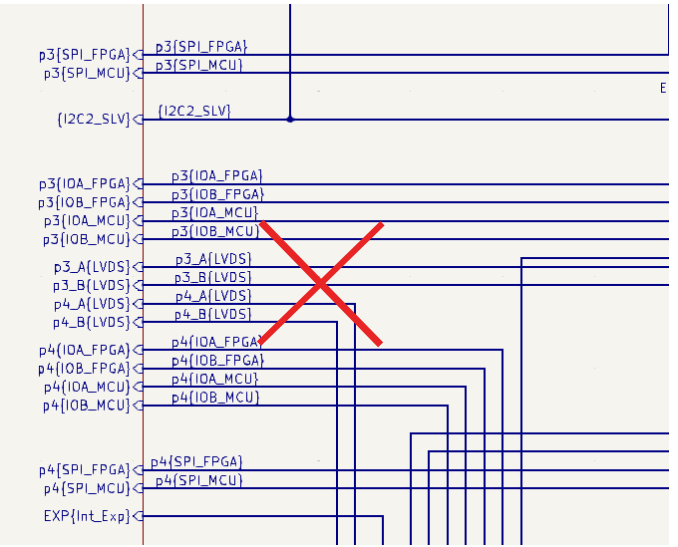
- Fixed in Sheet Properties:
  - Sheetfile should be the same
  - Sheetname should be different



ERCE_DUPLICATE_SHEET_NAME

Careful with busses

- Complex to use
- Will raise lots of ERC
- Use only if:
  - ≥ 4 signals
  - That need to go in > 2 places

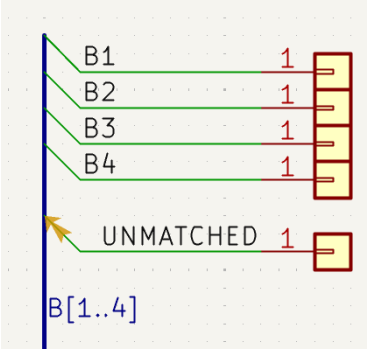


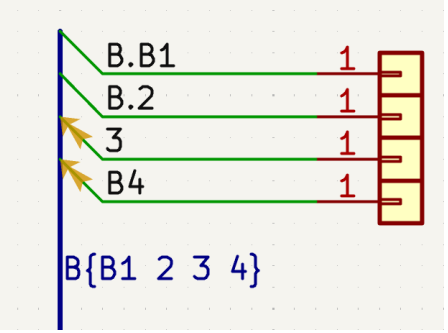
3 Get rid of ERCE

Bus entry issues

"Net X is graphically connected to bus Y
but is not a member of that bus"

- Bus label syntax is wrong
- Net name does not match bus label "regex"

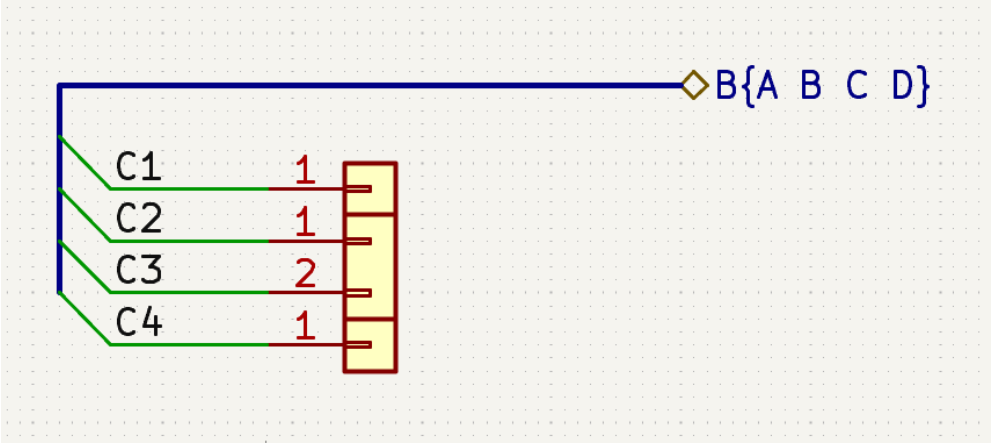




ERCE_BUS_ENTRY_CONFLICT

Bus entry issues issue

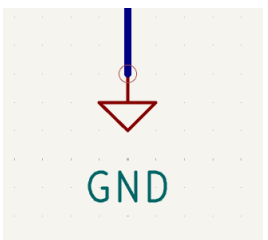
- “Bus entry issue” ERC not raised in daughter sheets (V9)
  - Bug #19646 recently fixed
- Check your “Label Not Connected” issues instead

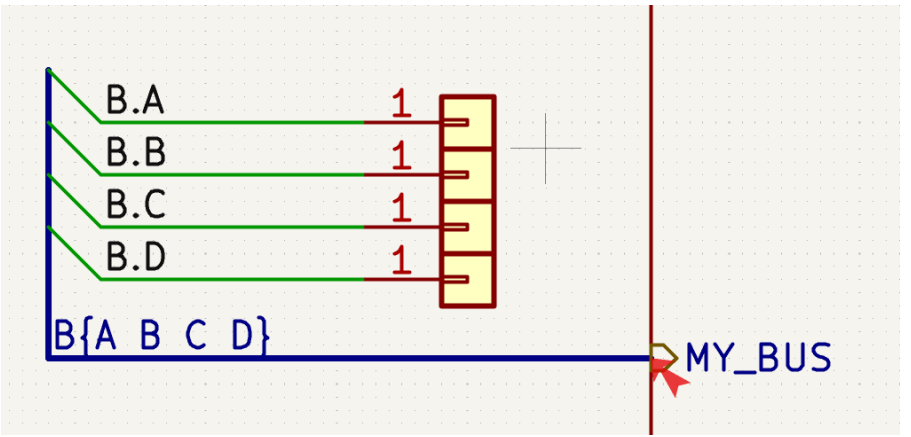


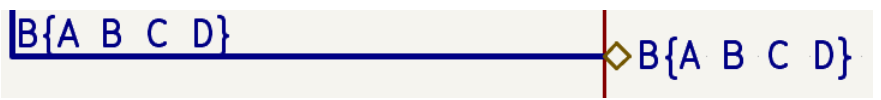
Bus to net conflict

"Invalid connection bus and net items"

- Bus name and hierarchical port name are different
- Something weird with power symbol (rare)





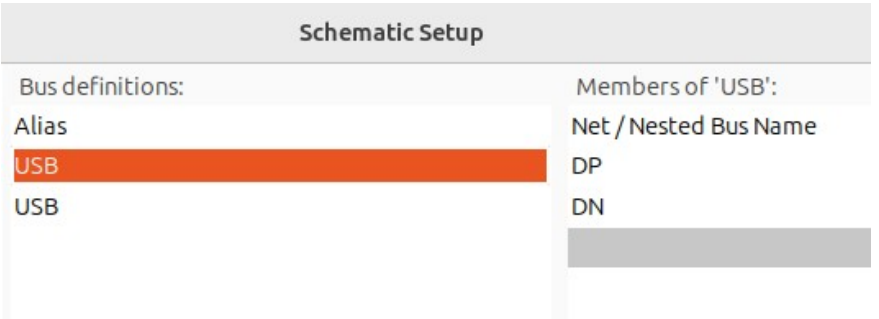


ERCE_BUS_TO_NET_CONFLICT

Bus alias definition conflict

"Bus alias X has conflicting definitions on sheet1.kicad_sch and sheet2.kicad_sch"

- Bus aliases are variables stored in kicad_sch files
- 2 schematics can have the same bus alias defined
- Remove one of the definitions from a schematics in Schematic Setup → Bus Alias Definition

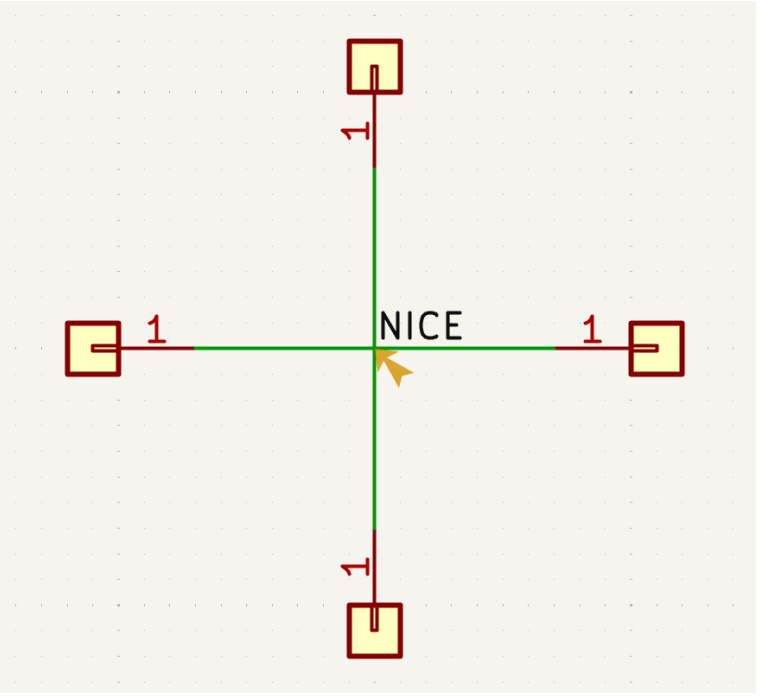


ERCE_BUS_ALIAS_CONFLICT

How do you even?...

“Label connects more than one wire“

- Label on multiple wires
- Happens when the label "hitbox" is on a non-connected intersection

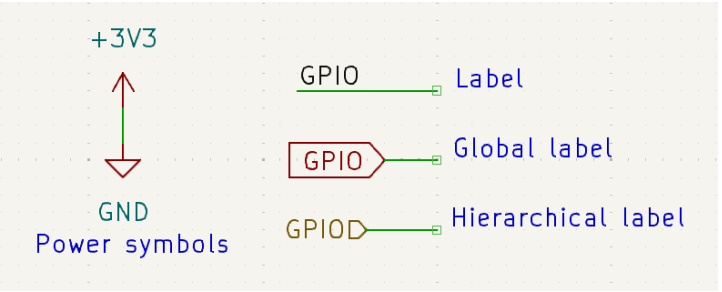


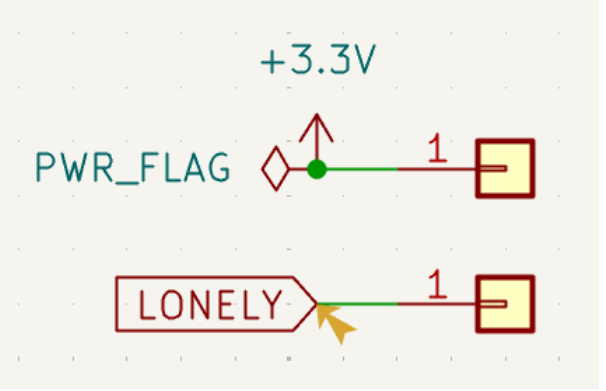
ERCE_LABEL_MULTIPLE_WIRES

Global labels not connected

"Global label not connected anywhere else in the schematics"

- Lonely global labels will trigger an ERC
- Lonely power symbols will not





ERCE_SINGLE_GLOBAL_LABEL

4- Pin types ERC

The “Power Input needs Power Output” ERC

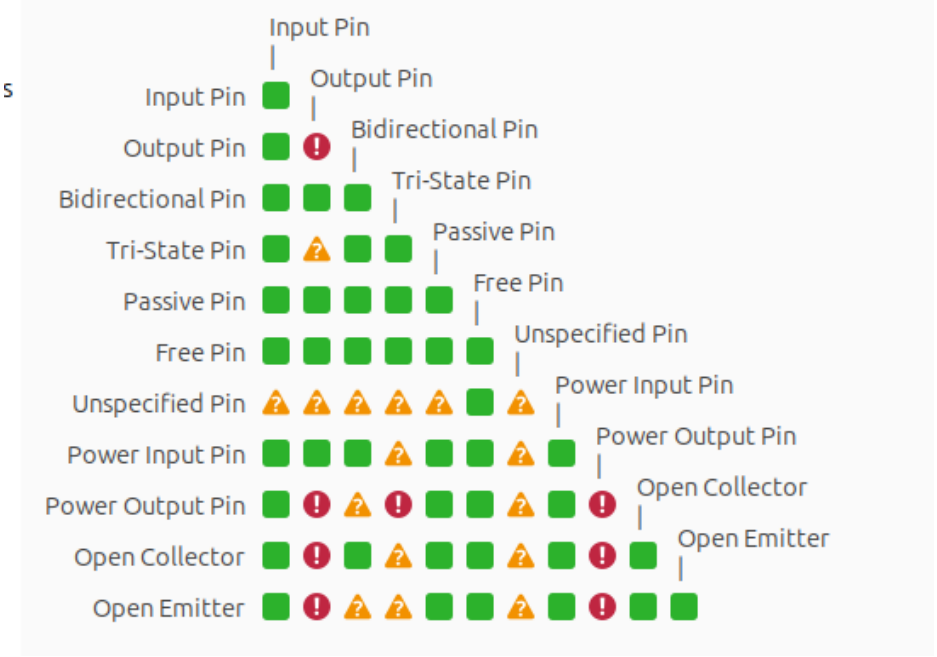
and the Dreaded Connection Matrix

Connection Matrix

Each symbol pin or hierarchical label has a type

- Some types are not compatible with one another
  - Outputs x Outputs 

- “Pins of type X and Y are connected”
  - Goal: avoid conflicts
  - Still not a SPICE simulation!

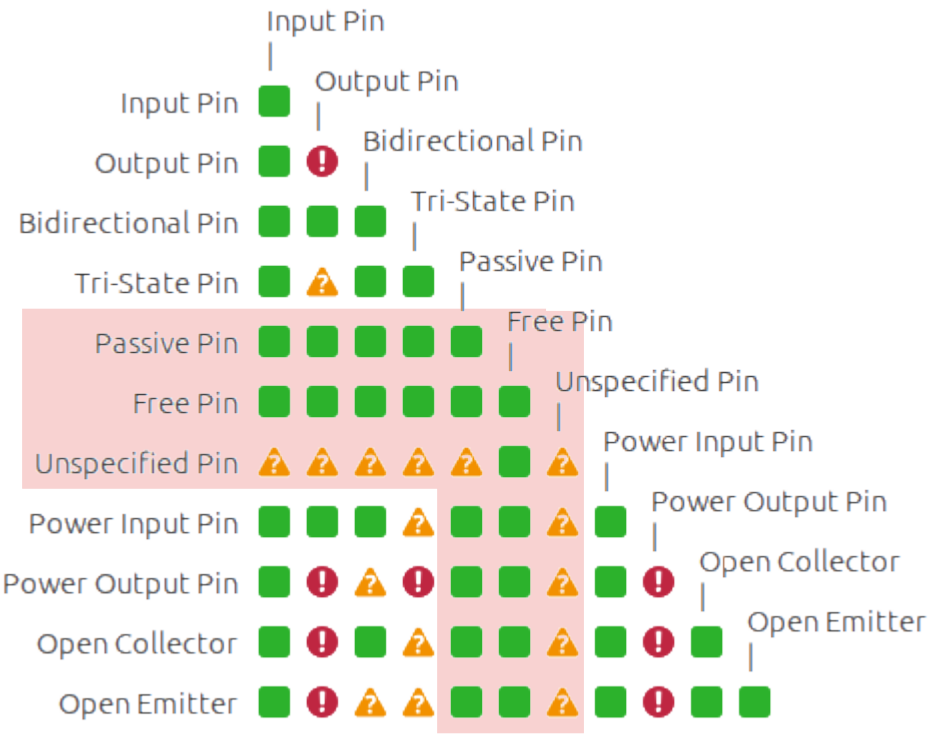


4 Pin types ERC

Special pin types

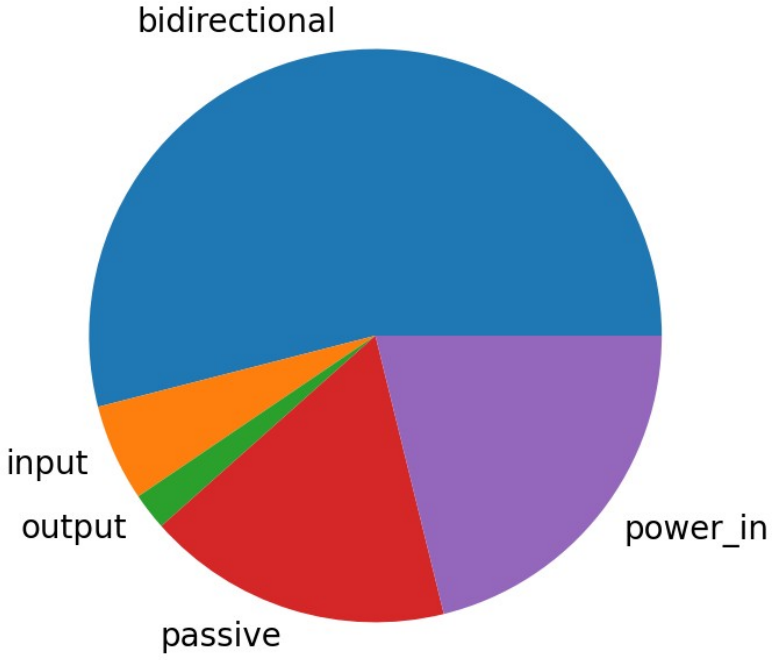
- “Unspecified” always gives warnings
- “No connect” can never be connected
- “Free” never gives warnings, but can be connected. Can be used for no-connect pins
- “Passive” is ideal for non-driven pins (connectors, passive components…)

All explained in :
https://docs.kicad.org/9.0/en/eeschema/eeschema.html#pin-electrical-types



Pin types popularity contest

bidirectional	282556
power_in	110717
passive	90425
input	28665
output	10924
no_connect	4259
power_out	2896
tri_state	1633
open_collector	1565
open_emitter	113
unspecified	33
free	25



KiCAD V8 standard library pin types (<1% hidden)

Special ERC for inputs

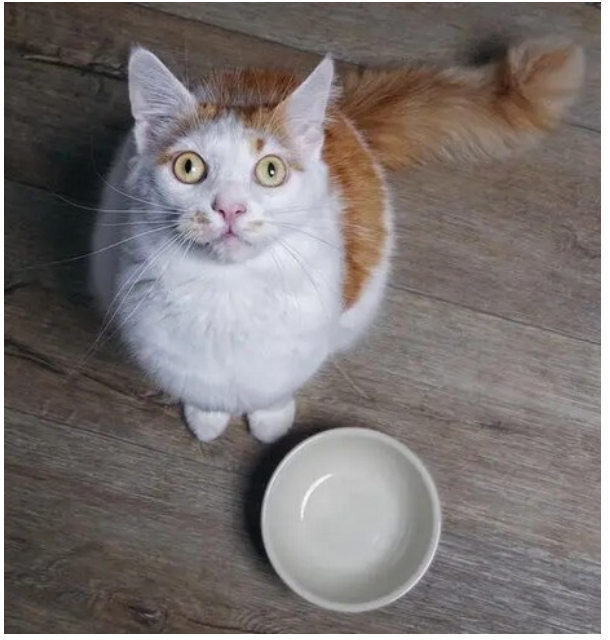
Input pin types are special!

- Input pins : need to be driven
  - Output
  - Power output
  - Passive
  - 3-State
  - Bidirectionnal

  « Input pin not driven by any output pins »

- Power input pins : need to be driven
  - Power output only

  « Input power pin not driven by any power output pins »

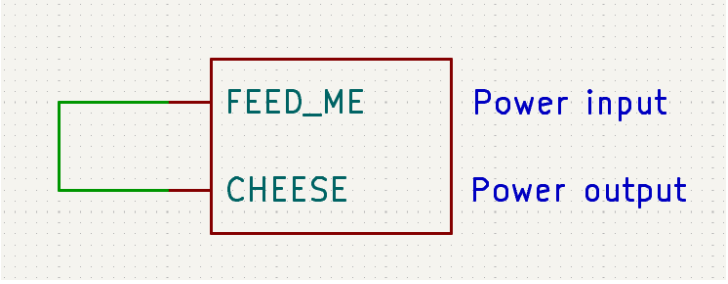


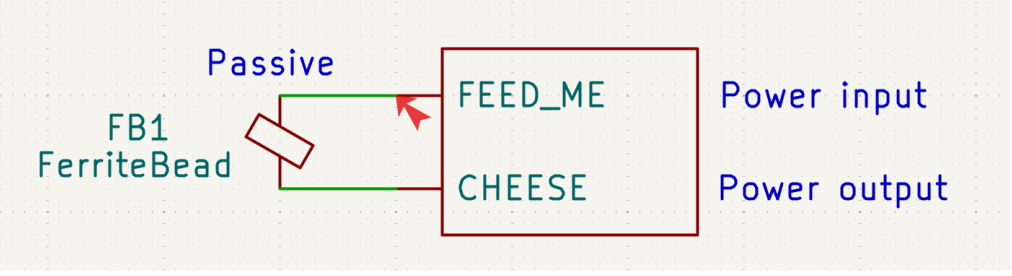
ERCE_PIN_NOT_DRIVEN
ERCE_POWERPIN_NOT_DRIVEN

Power input issue #1

"Input power pin not driven by any output power pins"

- What about power from passive pins (ferrites, connectors…)?
- What about third-party, non-optimal libraries?

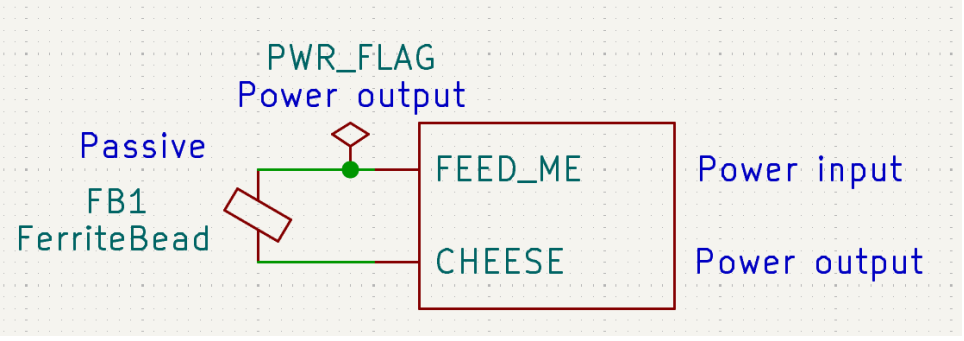




Power output flag

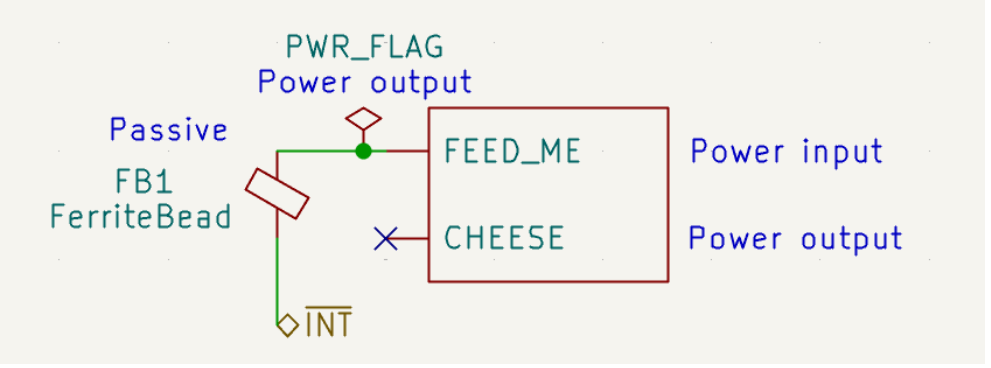
Add the Power Output flag!

- But not randomly
- Add it where the power comes from



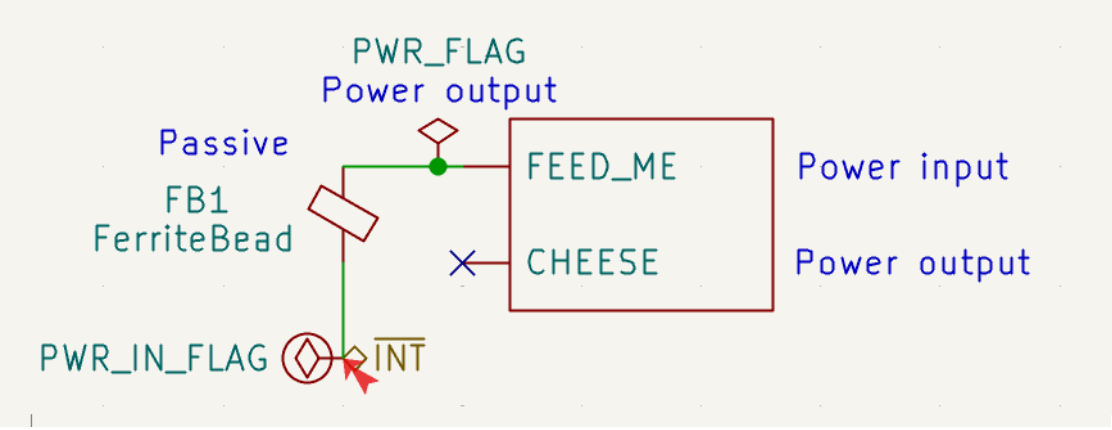
Power input issue #2

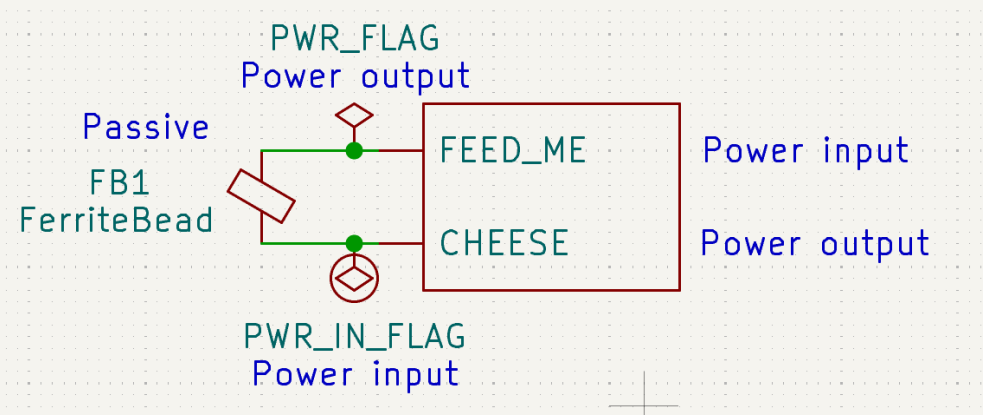
- Now the PWR_FLAG hides an issue...
- The ferrite not being supplied by any power output



Power input flag

- Create a custom Power Input Flag!
- It's just a component with a power input pin
  Tip : Uncheck the "power symbol" option

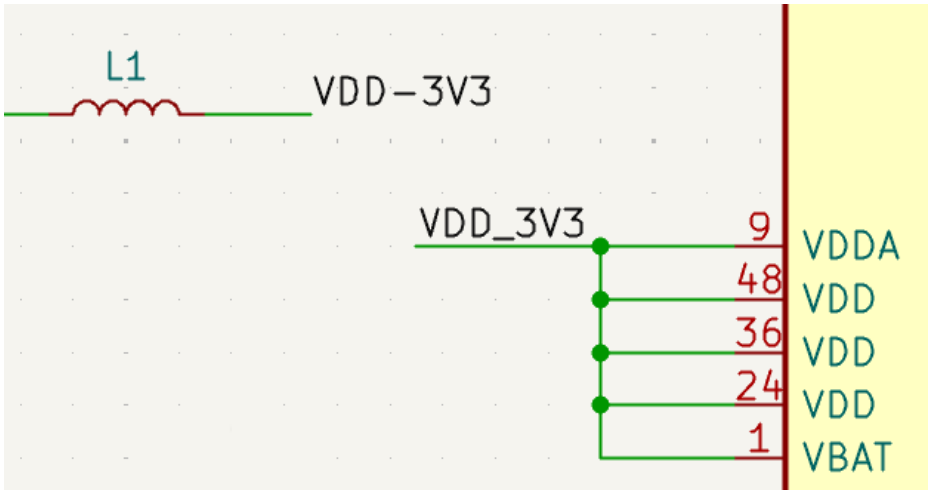




5 - ERC versus real life issues

+ Quizz: guess the ERC

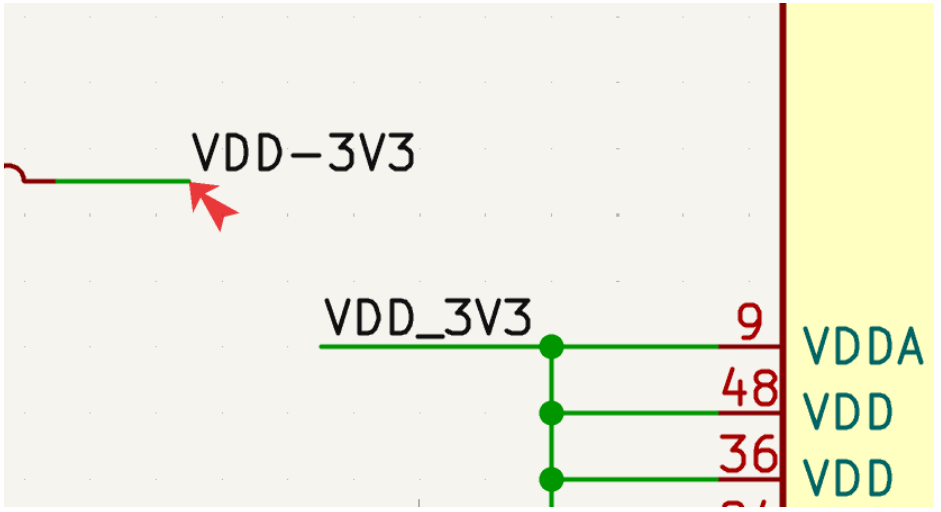
#1 Power supply typo



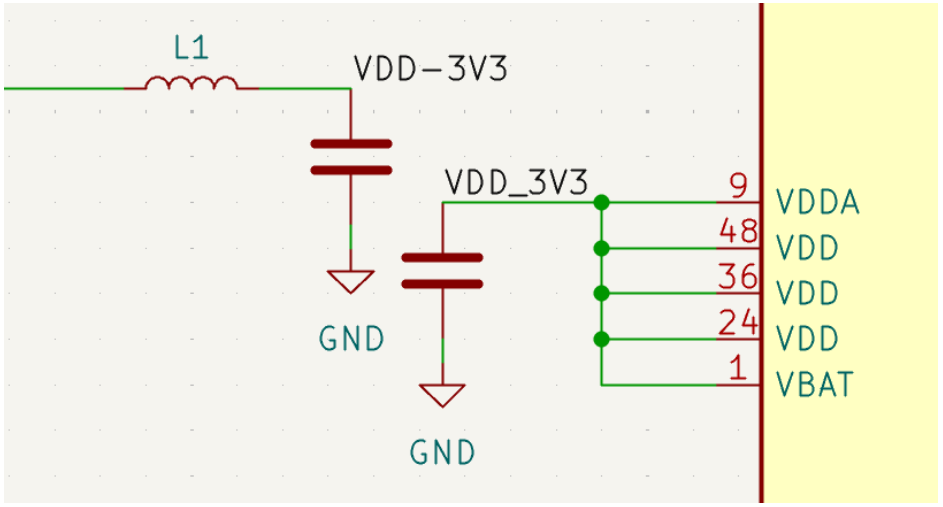
Which ERC will pop in this case?

#1 Power supply typo

"Label not connected to anything"



#1 Power supply typo

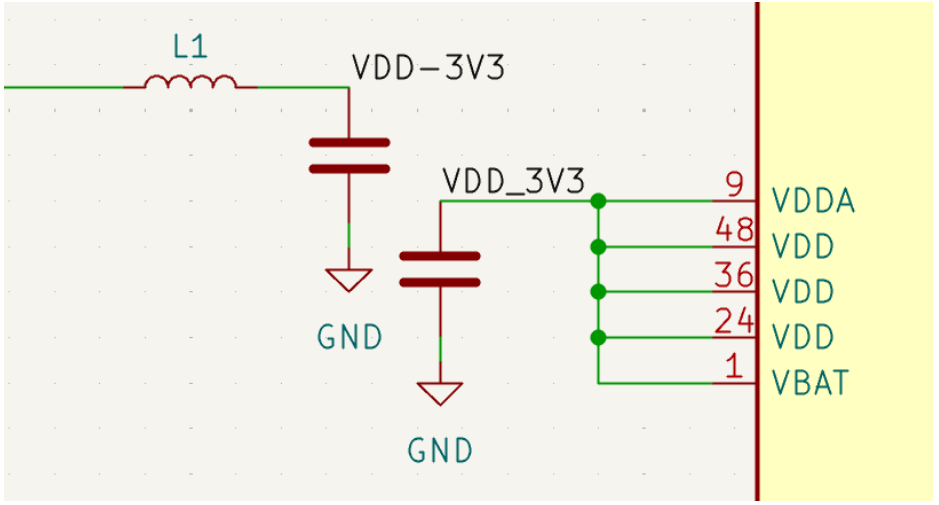


Which ERC will help now?

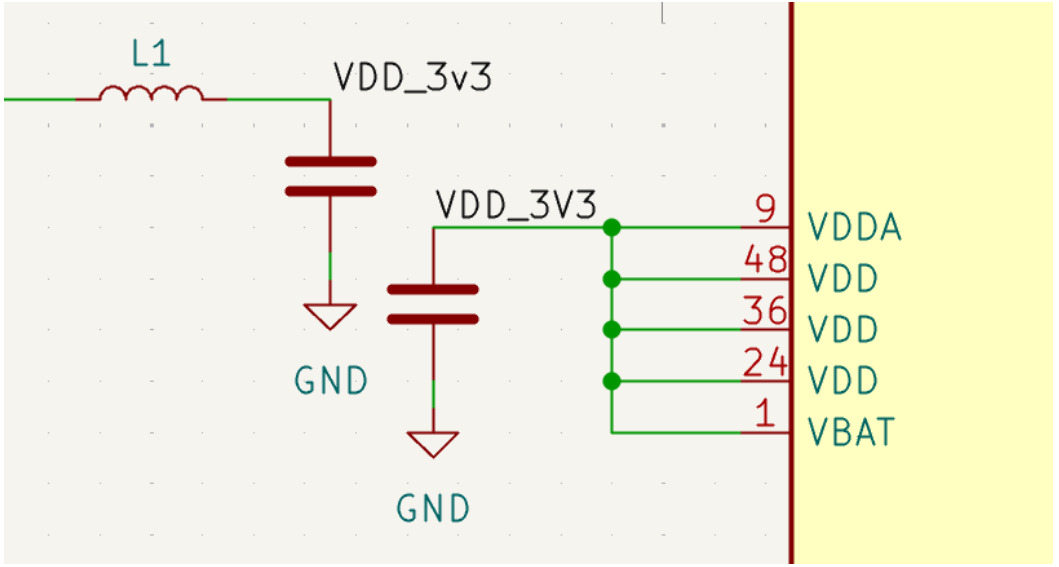
#1 Power supply typo

"Input power pin not driven by any output power pins"

- VDD pins are power input, without a power output!



#1 Power supply typo



What about now?
Another cool ERC maybe?

Suspected typos

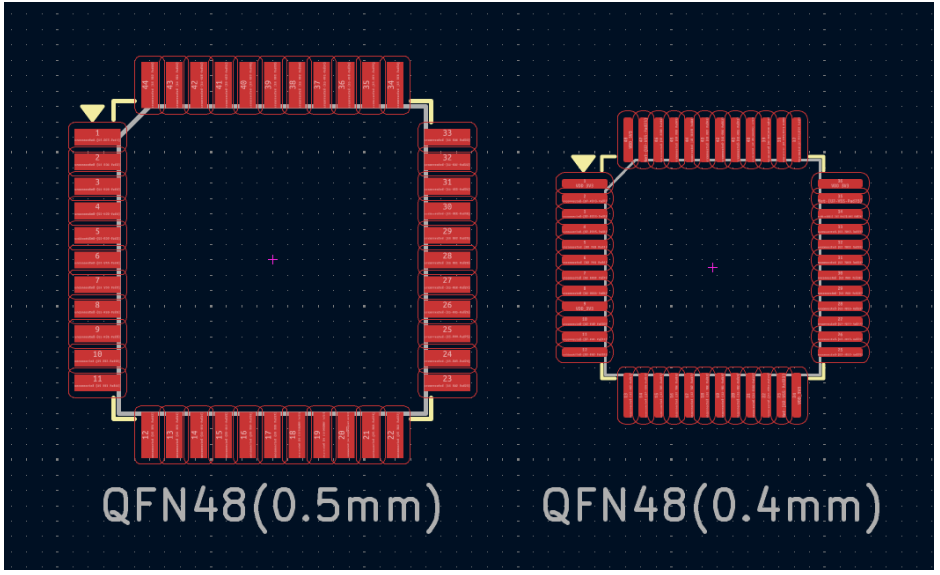
- KiCAD is case-sensitive
  3v3 is not 3V3
- ERC only catching case oopsies

ERCE_SIMILAR_LABELS	2 labels are equal for case insensitive comparisons.
ERCE_SIMILAR_POWER	2 power pins are equal for case insensitive comparisons.
ERCE_SIMILAR_LABEL_AND_POWER	Label and pin are equal for case insensitive comparisons.
ERCE_SAME_LOCAL_GLOBAL_LABEL	2 labels are equal for case insensitive comparisons.

#2 Footprint mismatch

- Wrong footprint on an IC
  - The trap: QFN pitch
  - Read datasheet carefully

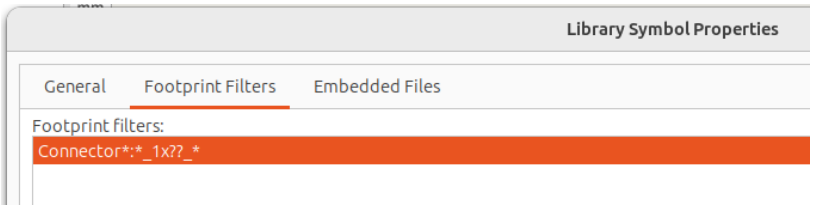
Do you know an ERC
that could help?



Footprint filters

"Assigned footprint X doesn't match footprint filters "

- Footprint filter
  - Simplified regex, only * and ?
  - Defined in symbols
  - Different from the "Footprint" field
  - ERC disabled by default



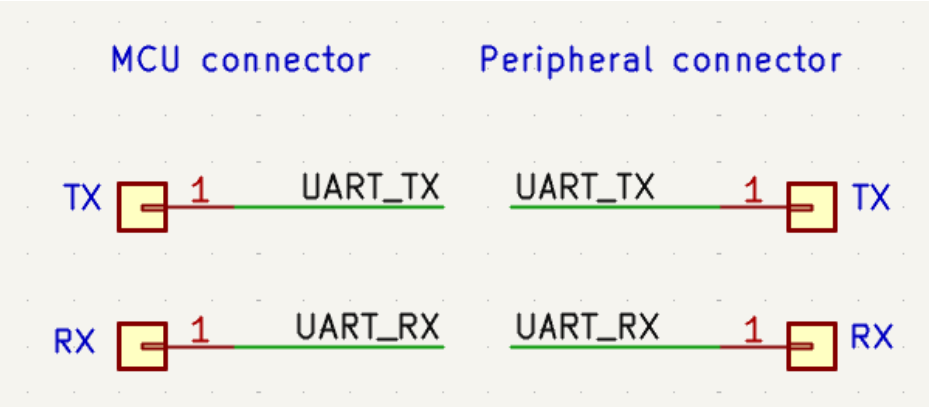
Example STM32F722ICTx:

- Footprint: LQFP-176_24x24mm_P0.5mm
- Filter: LQFP*24x24mm*P0.5mm*

TX / RX inversion issues

Infinite variations on a theme

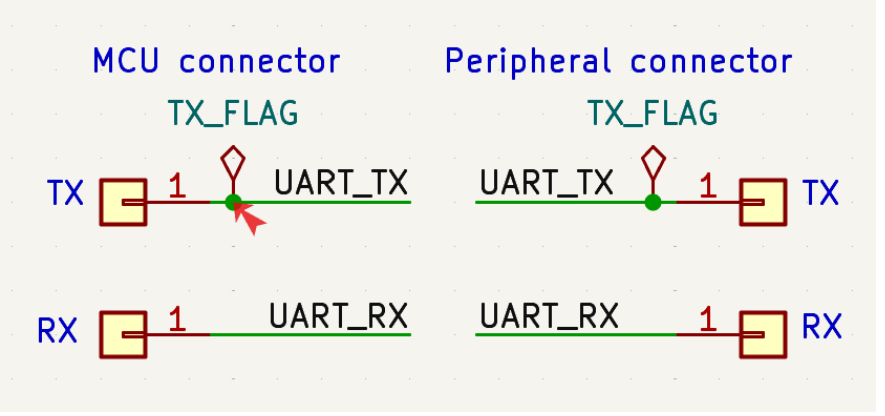
- Simply forgotten
- Split on different pages
- Interverted several times

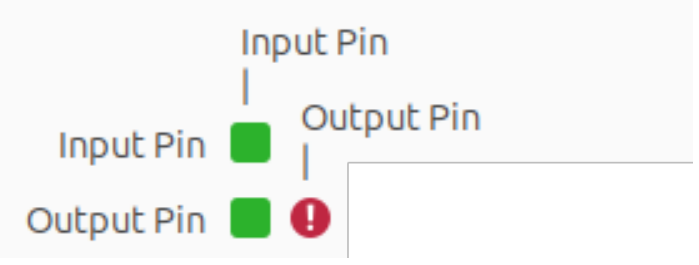


What could we do?

#3 TX / RX inversion issues

- Rename them MCU_TO_PERIPHERAL / PERIPHERAL_TO_MCU
- Create an “Output Pin” flag to flag TX
  - 2 output pins are exclusive
  - Inversion issue : “Pin of type Output and Output are connected”
- Use the alternate pin feature!

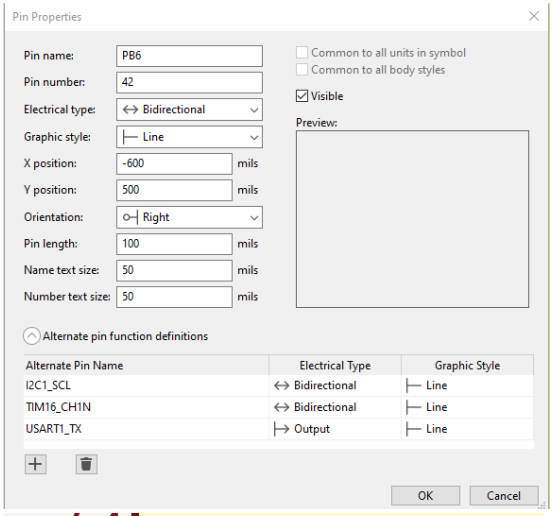


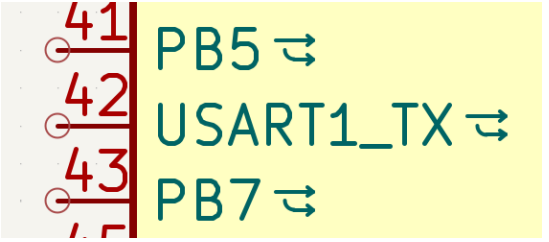


TX/RX inversion issues

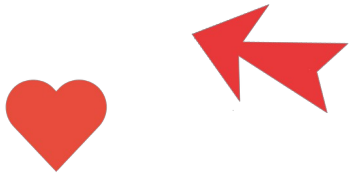
New feature in V9:

- Alternate pins set up in symbol
- Each alternate can have its own electrical type
- Change your TX alternate to “Output“!

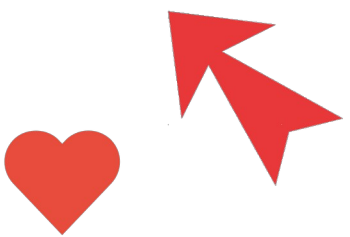




Conclusion



- Learn to use all the ERC you can!
- Clean up all the noise to be warned of anything suspicious!
- Analyze your mistakes and find ways to detect them!
- KiCAD is open-source: participate!



References

- Full documentation about ERC
  https://docs.kicad.org/9.0/en/eeschema/eeschema.html#list-of-erc-checks
- KiCAD bug tracker
  https://gitlab.com/kicad/code/kicad/-/issues
- Actually Useful Schematics in KiCAD, by Andrew Greenberg
  https://www.youtube.com/watch?v=X0hd_v8qRiY
- Popularity contest for QFN/QFP pitches
  https://www.flashpcb.com/blog/QFP-QFN-Miniaturization

Thank you !!! ❤

Question time !