aesc

ElemRV

Open-Source RISC-V Microcontroller

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January 31st

aesc silicon

Introduction & History

What is ElemRV?

- A collection of **end-to-end open-source** RISC-V Microcontrollers
- Multiple platforms are available based on **Element names**
- Name combines **"Elements"** and **"RISC-V"**
- Fully implemented in **SpinalHDL**
- Licensed under **CERN-OHL-W-2.0**
- Supports both FPGA and ASIC implementation workflows

IHP: Innovations for High Performance Microelectronics

About IHP:

- Publicly funded research institute focused on silicon/germanium electronics
- Operates pilot line manufacturing circuits using high-performance SiGe BiCMOS technologies
- Located in Frankfurt (Oder), Germany

Key Fundings:

- 130nm Open-Source PDK
- Free MPW (Multi-Project Wafer) runs to validate analog and digital components

First Tape-Out (May 2024)

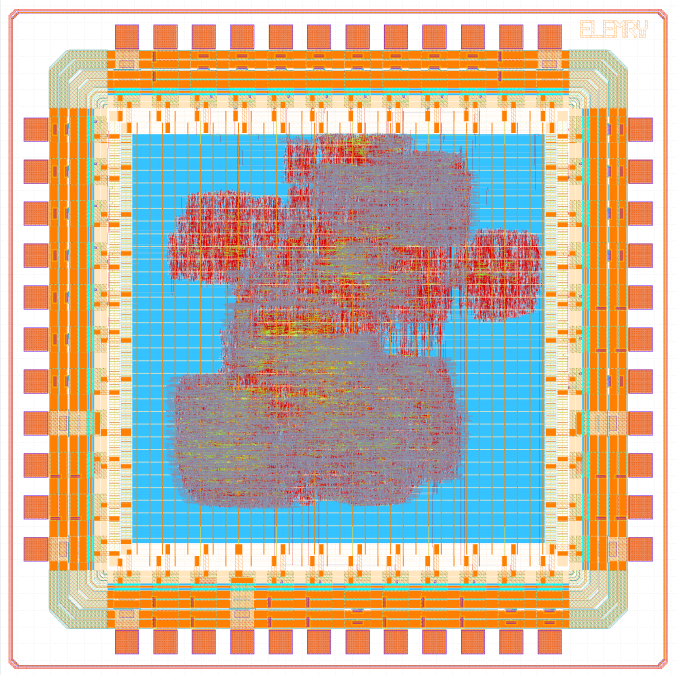
Opportunity to validate the PDK with a digital design

Design Approach:

- Leveraged existing FPGA-based design
- HyperBus interface for external memory

Design Philosophy:

- **Conservative:** focus on bootable silicon
- PDK was in alpha stage – stability was priority



First Tape-Out Layout (May 2024)

Silicon Bring-up (February 2025)

Received silicon in **February 2025**

Results:

- One bug discovered: HyperBus interface prevents running data and instructions in external memory
- Despite bug, achieved **first booting silicon** with IHP's Open PDK
- Core functionality validated

Significance:

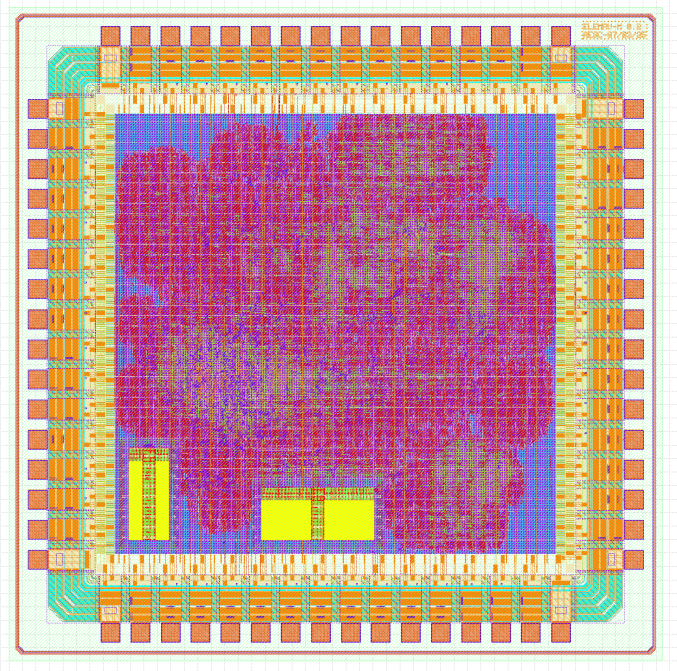
- Open-source silicon with no NDA requirements

Second Tape-Out (April 2025)

Improvements:

- Fixed HyperBus interface
- Added **On-Chip RAM** for better performance
- Expanded IO interfaces
- Pinmux Controller
- Integrated **Masked AES** for side-channel attacks

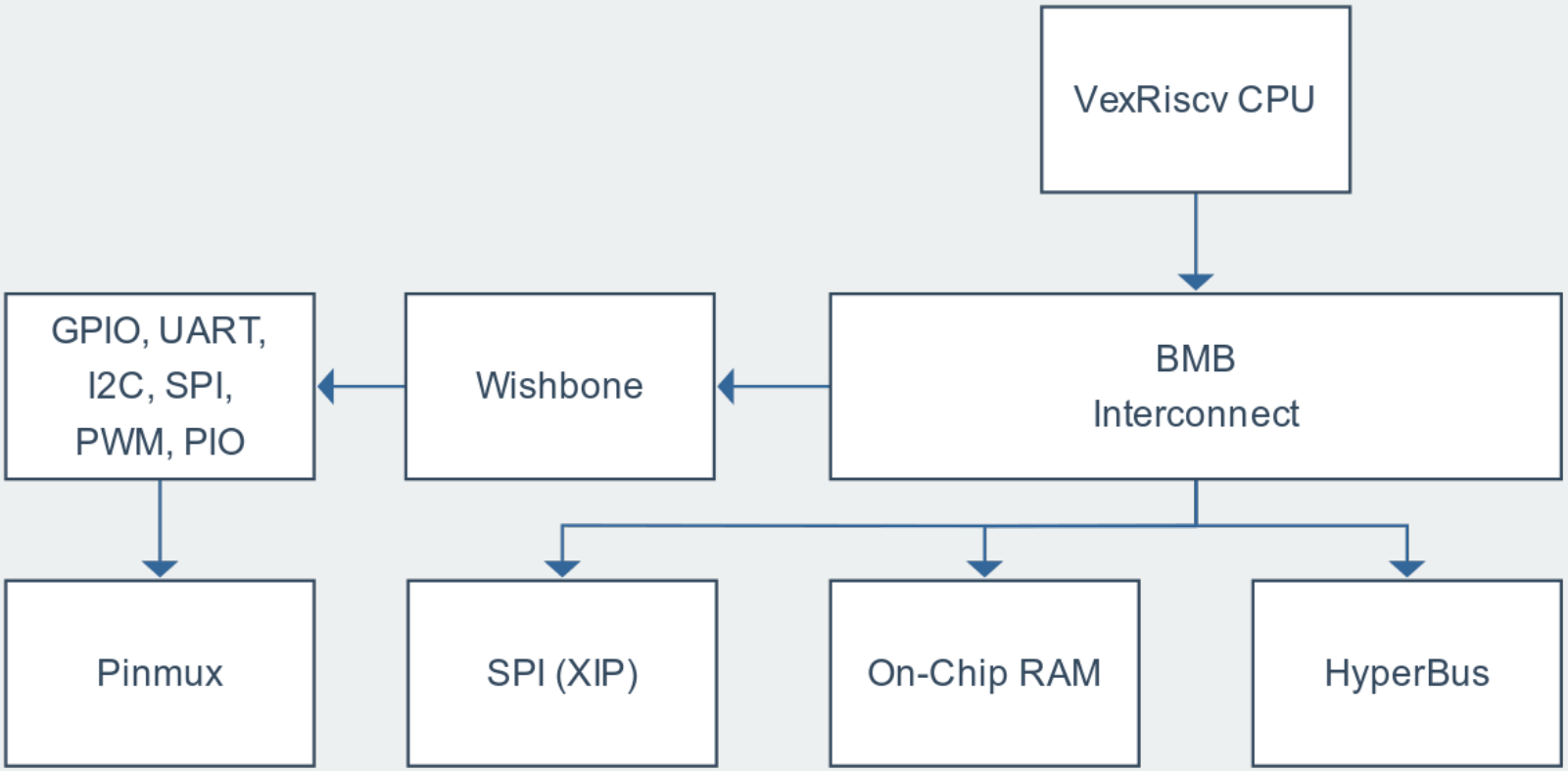
Status: Awaiting silicon delivery



Second Tape-Out Layout (Apr 2025)

Architecture

Overview Nitrogen



VexRiscv

32-bit RISC-V CPU with a 5-stage pipeline

- CPU fully written in SpinalHDL
- Plugin-based architecture
- RV32IMCZicsr instruction set:
  - **I** – Full Integer base extension
  - **M** – Hardware multiply and divide
  - **C** – Compressed instructions (16-bit)
  - **Zicsr** – Control and Status Register (CSR)

BMB/Wishbone Bus

What's wrong with AXI4/APB3?

- AXI4 is too complex for small, simple designs
- Specification is hard to implement
- Open Specification but still licensed by Arm

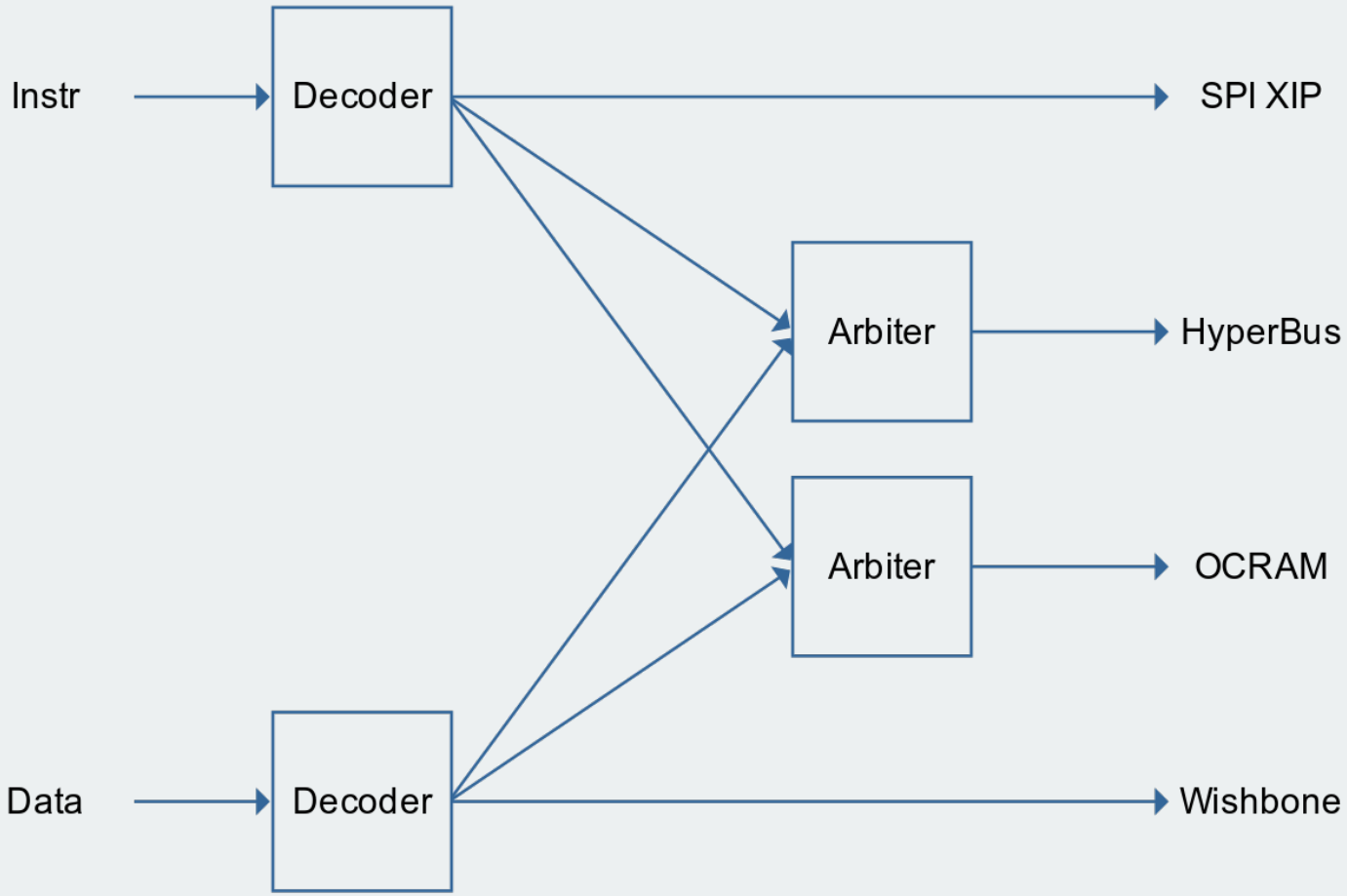
Banana Memory Bus (BMB)

- Written by Charles Papon (SpinalHDL)
- Command and Request channels architecture
- Replacement for AXI4 crossbar

Wishbone

- BMB is point-to-point only
- Wishbone supports shared subordinates
- Replacement for APB3

BMB/Wishbone Bus



SPI XIP Controller

The Challange: SPI flash devices require a specific communication protocol for memory access (command, address, dummy cycles, data)

Dual-mode Controller:

- Standard SPI controller for general transactions
- XIP controller for transparent flash memory access

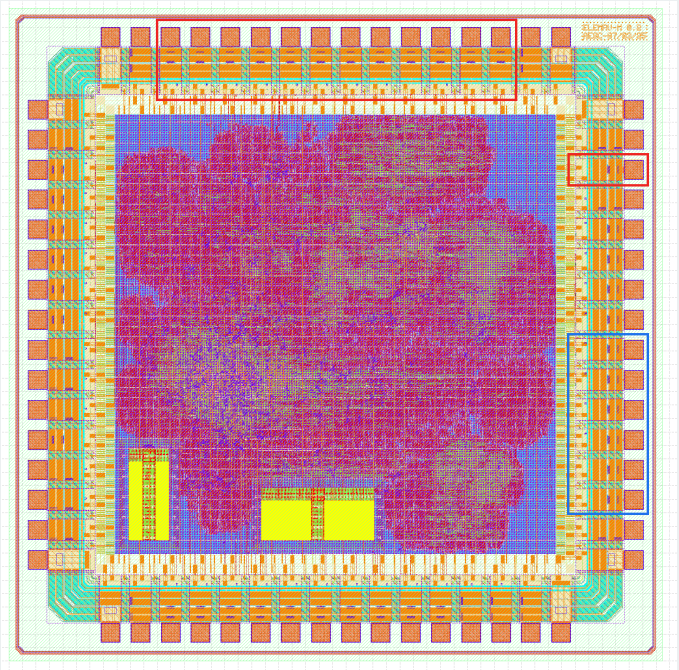
Features:

- Runtime-switchable I/O protocols
- Supported modes: Standard (1-bit), Dual (2-bit), Quad (4-bit)
- Higher bandwidth with multi-bit protocols

HyperBus

Problem: External static memory is expensive and SDRAM is complex for small microcontroller designs.

- Octa SPI like interface
- Low-IO count (11 + chip-select)
- HyperRAM and HyperFLASH devices available
- Memory and flash on the same interface
- Throughtput with up to 800 MB/s

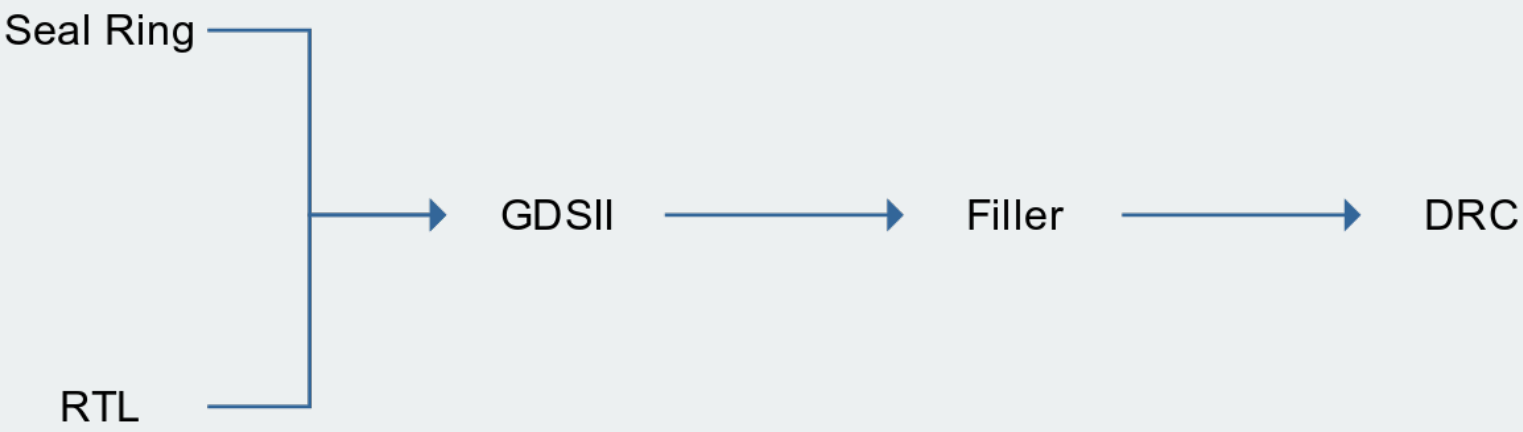


Red: HyperBus interface

Blue: SPI interface

ASIC Flow

ASIC Flow - Overview



RTL

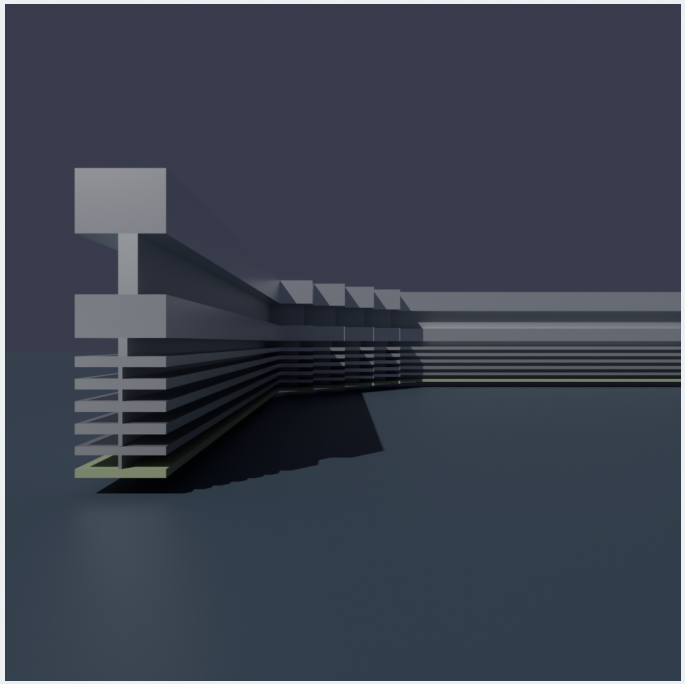
- EDA tools only understand Verilog/VHDL.
- ElemRV is fully written in SpinalHDL.
- A Scala-based framework for generating Verilog/VHDL
- Enables high-level hardware description with modern programming constructs

```
1 val reg = Reg(UInt(4 bits)) init(0)
2 when (tick) {
3   reg := reg + 1
4 }
5 def doSomething = reg === U(5)
```

Seal ring / Guard ring

Ring around the entire chip using all layers in the metal stack.

- Blocking ionic contamination
- Reduce mechanical stress during die sawing
- Stopping cracks from the chip edge
- Prevention of moisture

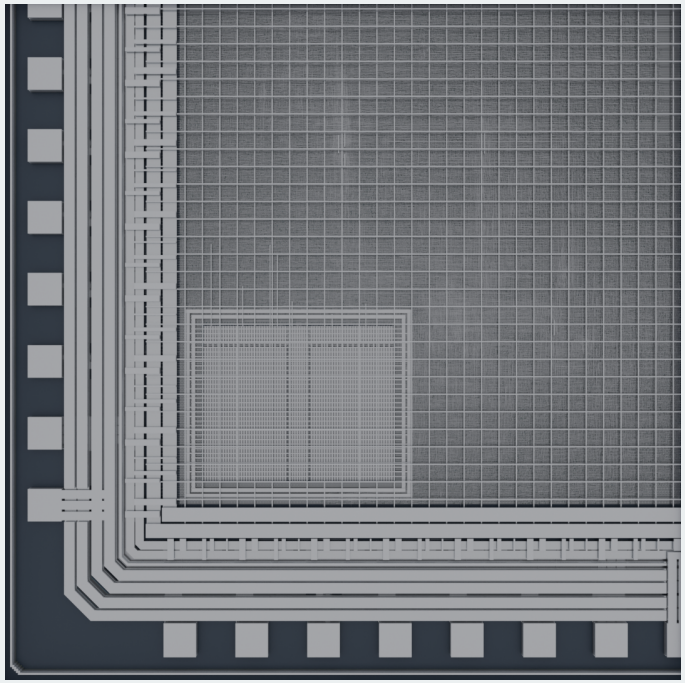


IHP SG13G2 Sealring

GDSII Layout

Convert RTL code to a GDSII layout.

- RTL to netlist synthesis
- Floorplanning and power grid
- Placement of standard cells
- Clock tree synthesis (CTS)
- Global and detailed routing
- Parasitic extraction and timing
- Physical verification and signoff



GDSII Layout

Filler

The Challenge:

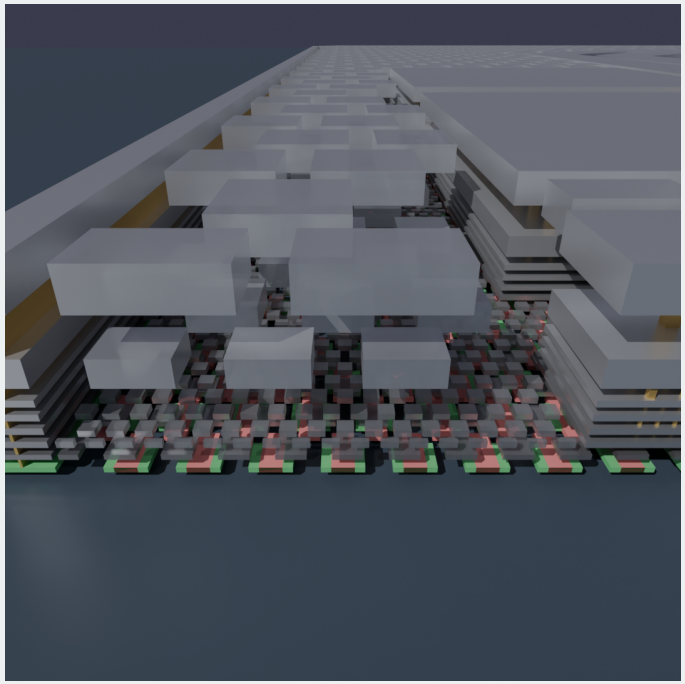
Non-uniform metal density affects chemical-mechanical polishing (CMP) during fabrication.

Why This Matters:

- Uneven polishing causes thickness variations
- Results in unpredictable electrical characteristics

The Solution:

- Insert dummy metal fill patterns



GDSII with metal dummy fill

Design Rule Check (DRC)

DRC verifies that the layout complies with all foundry-specific design rules before fabrication.

- Foundry provides comprehensive design rule deck
- EDA tools perform automated checks but may miss complex interactions

Example:

- Spacing violations between metal layers can cause shorts

5.22 TopMetal1

Rule	Description	Value
TM1.a	Min. **TopMetal1** width	**1.64**
TM1.b	Min. **TopMetal1** space or notch	**1.64**
TM1.c	Min. global **TopMetal1** density [%]	**25.00**
TM1.d	Max. global **TopMetal1** density [%]	**70.00**

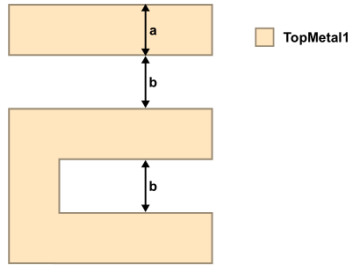


Figure 5.22: TopMetal1 dimensions

Source: IHP-Open-PDK SG13G2 Layout Rules[1]

[1] https://github.com/IHP-GmbH/IHP-Open-PDK

Taskfile

task prepare

- Generates Verilog source files
- Produces all required OpenROAD artifacts
- Creates a seal ring macro

task layout

- Generate the final GDSII layout

task filler

- Inserts filler cells to all required layers

task run-drc [level=minimal]

- Performs Design Rule Checks (DRC)

What's Next?

Open-Silicon MPW Shuttle with IHP Open PDK

First Open-Silicon MPW Service Using IHP Open PDK

Pricing:

- **1500€ per mm²** for open-source designs

Upcoming Tape-Out Dates:

- **March 30, 2026** – SG13CMOS
- **July 13, 2026** – SG13CMOS5L
- **October 6, 2026** – SG13G2

Register Now

Scan for registration

More info:

`https://dk.ihp-microelectronics.com/OpenSourceRequest.php`

Tape-out March

$7\,\mathrm{mm}^2$ are reserved on IHP's first open-source MPW shuttle in March 2026.

Planned features:

- Improve HyperBus performance
- Add small CPU caches based on SRAM blocks
- Introduce partitions with optimized clock frequencies

BlenderGDS: Visualizing Silicon

What is BlenderGDS?

- Blender Add-on for importing **GDSII files**
- Generate high-quality 3D renders of chip layouts
- Perfect for presentations, publications, and documentation

Scan to visit BlenderGDS

More info: `https://github.com/aesc-silicon/BlenderGDS`

Get Involved

ElemRV is Open-Source

License:

- CERN-OHL-W-2.0 (Hardware)
- Permissive open-source license

How to Contribute:

- Report issues and bugs
- Submit pull requests
- Request features

Scan to visit ElemRV

More info: `https://github.com/aesc-silicon/ElemRV`

Thank You!

Available for Contract Work!

Contact:

- Email: `daniel@aesc-silicon.de`
- GitHub: `github.com/aesc-silicon`
- LinkedIn: `linkedin.com/in/dnltz`

Daniel Schultz

Questions?

Bonus

Peripheral Design: IP Identification

Every peripheral includes an **8-byte IP Identification block** at the start of its register map:

Identification Fields:

- **API Version** – Interface compatibility level
- **Block Length** – Size of register space
- **Unique IP ID** – Identifies peripheral type
- **Version Numbers** – Major, minor, and patch

Field	Offset
API Version	0x00
Block Length	0x01
IP ID	0x02-0x03
Major Ver	0x04
Minor Ver	0x05
Patch Ver	0x06-0x07

8-byte ID block structure

Peripheral Design: IP Capabilities

Following the IP identification, each peripheral provides a **capabilities register block** that describes its configuration.

Why Capabilities?

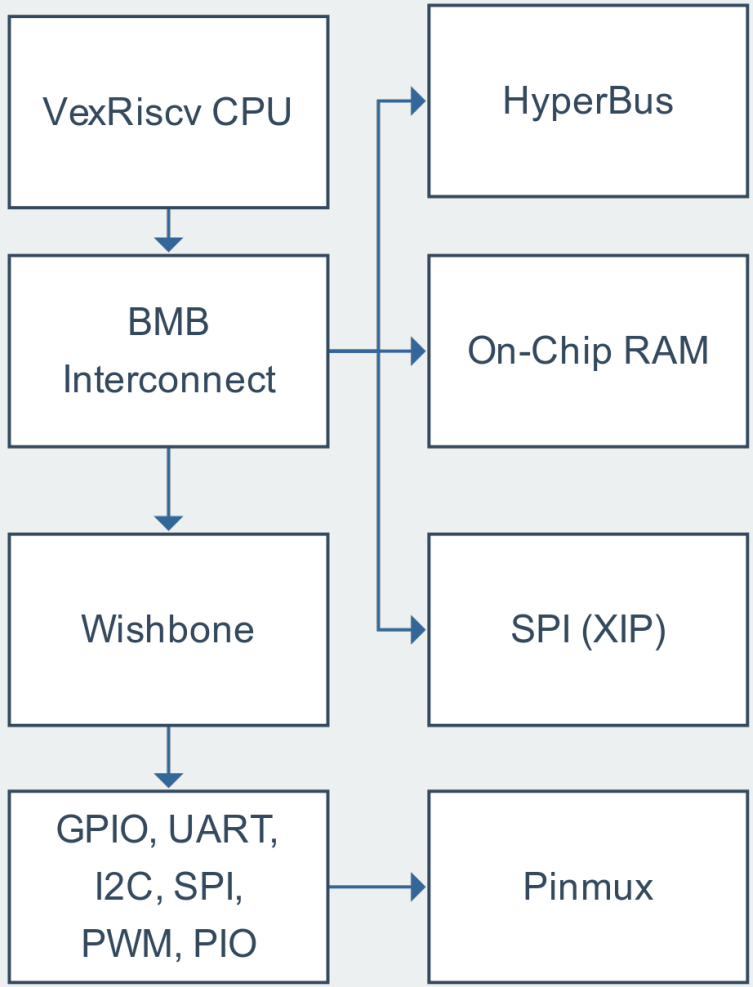
- Drivers adapt to actual hardware
- Single driver supports multiple configurations
- No compile-time hardware assumptions

Example: PWM

- Amount of channels
- Period register width
- Pulse register width

Overview ElemRV-N

- 64 Pins
- 100 MHz input clock
- Asynchronous design
- RISC-V RV32IMCZicsr
- External HyperRAM
- 4kB On-Chip RAM
- External SPI flash
- 20 muxable pins



Overview ElemRV-H

- 32 IO Pins
- 50 MHz input clock
- synchronous design
- RISC-V RV32IMCZicsr
- 8kB On-Chip RAM
- External SPI flash
- 12 muxable pins