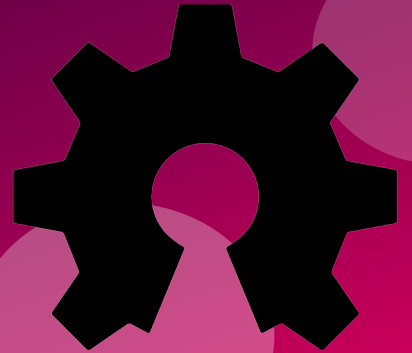


Sucr LA

Open source, USB 3.0, FPGA based
logic analyzer

Yann Sionneau
FOSDEM 2026



open source
hardware

Menu

- Me
- Wait, wat?!
- Why this project?
- (current) Target specifications
- What has been done so far
- What next?
- *“Bon appétit !”*

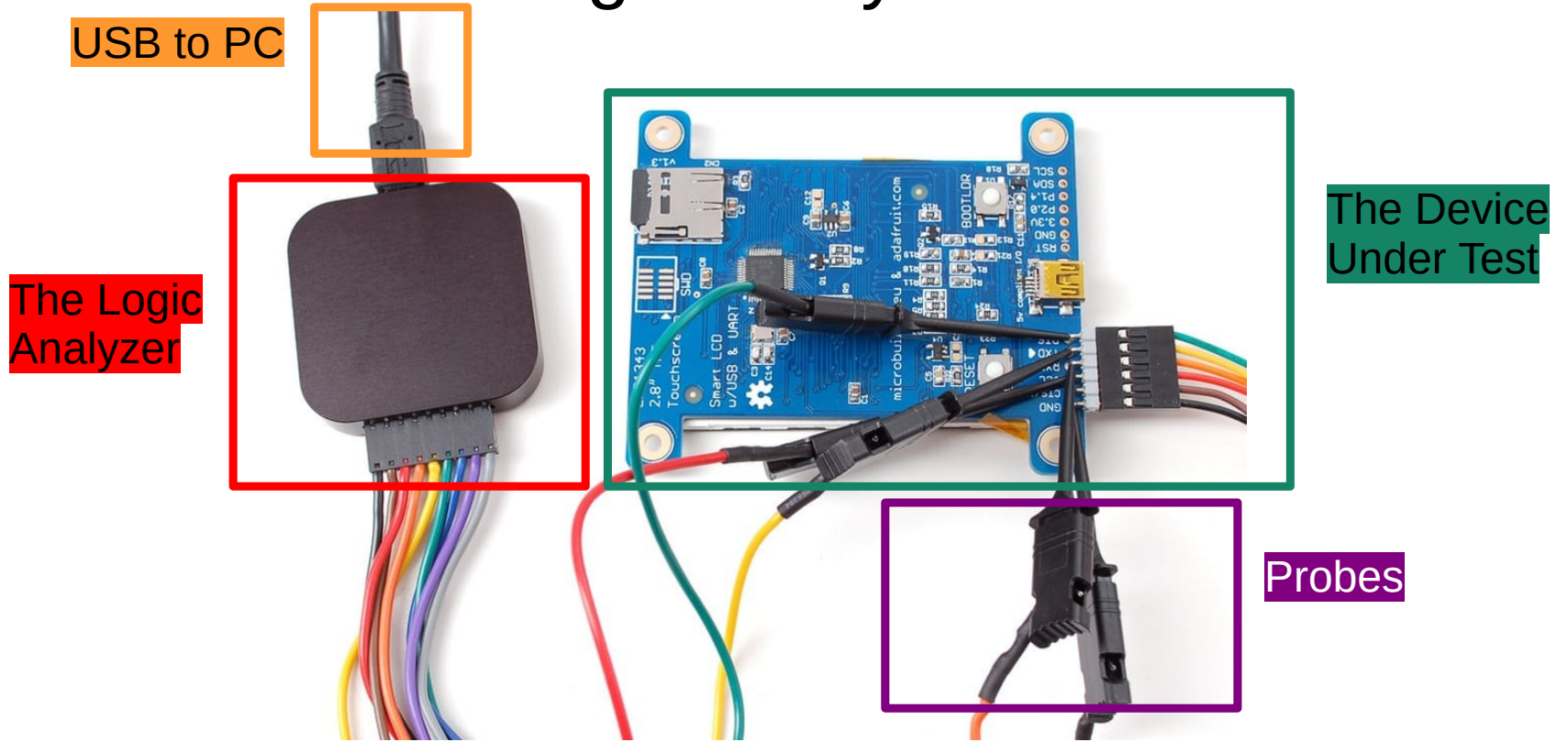
Me

Yann Sionneau
French 🍞, from Grenoble 🏔️
37 years old

Kernel & Hypervisor engineer @ Vates
A French company that makes an open-source hypervisor
based on *Xen* called *XCP-ng*

Sucr LA, what is it?

A Logic Analyzer



SucréLA, what is it?

- USB 3.0
- FPGA based
- Open Source

SucréLA, wait... wat?!

SucréLA: pronounce “*Sucré*” (in French) *LA* (like *Los Angeles*)

bad pun based on “*Saleae*” (pronounced ... ??????)

It means “sweet” Logic Analyzer.

Yeah...no very funny...that's what happens when you explain a joke...

Saleae is a Logic Analyzer device vendor.

Why this project?

Make a *reasonably* fast, *reasonably* cheap, open source logic analyzer!

Why this project?

Most open source logic analyzers today:

Cypress FX2 based boards + fx2lafw open source firmware +
sigrok/PulseView host software



Why this project?

Most open source logic analyzers today:

Cypress FX2 based boards + fx2lafw open source firmware + sigrok/PulseView host software

USB 2.0

=> max real-time **streaming** sampling rate:
~24 to 48 Msps
(Note, there are others than fx2)



USB 3.0 solutions comparison

				Saleae Logic 16Pro
Real-time streaming				Yes
Sampling				100 Msps x16 400 Msps x4
Configurable threshold				No, 3 options: 0.6V, 0.9V, 1.65V
Firmware Gateway Board design				Closed source
Host soft.				Closed source
Price				\$1499

USB 3.0 solutions comparison

			Sipeed SLogic16U3	Saleae Logic 16Pro
Real-time streaming			Yes	Yes
Sampling			200 Msps x16 400 Msps x8 800 Msps x4	100 Msps x16 400 Msps x4
Configurable threshold			Yes 0V ~ 6V (0.1V step)	No, 3 options: 0.6V, 0.9V, 1.65V
Firmware Gateway Board design			Closed source	Closed source
Host soft.			Open source sigrok based	Closed source
Price			\$69	\$1499

USB 3.0 solutions comparison

		DreamsourceLab DSLogic U3Pro16	Sipeed SLogic16U3	Saleae Logic 16Pro
Real-time streaming		Yes	Yes	Yes
Sampling		125 Msps x16 500 Msps x6 1 Gsps x3	200 Msps x16 400 Msps x8 800 Msps x4	100 Msps x16 400 Msps x4
Configurable threshold		Yes 0V ~ 5V (0.1V step)	Yes 0V ~ 6V (0.1V step)	No, 3 options: 0.6V, 0.9V, 1.65V
Firmware Gateway Board design		Closed source	Closed source	Closed source
Host soft.		Open source (*) sigrok based	Open source sigrok based	Closed source
Price		\$299	\$69	\$1499

USB 3.0 solutions comparison

	Sucr�LA	DreamsourceLab DSLogic U3Pro16	Sipeed SLogic16U3	Saleae Logic 16Pro
Real-time streaming	Yes	Yes	Yes	Yes
Sampling	100 Msps x16 200 Msps x8 400 Msps x4	125 Msps x16 500 Msps x6 1 Gsps x3	200 Msps x16 400 Msps x8 800 Msps x4	100 Msps x16 400 Msps x4
Configurable threshold	Yes 0V ~ 3.3V (0.03V step)	Yes 0V ~ 5V (0.1V step)	Yes 0V ~ 6V (0.1V step)	No, 3 options: 0.6V, 0.9V, 1.65V
Firmware Gateway Board design	Open source	Closed source	Closed source	Closed source
Host soft.	Open source sigrok based	Open source (*) sigrok based	Open source sigrok based	Closed source
Price	??	\$299	\$69	\$1499

fx3lafw

- Open source firmware (like fx2lafw)
- With sigrok driver
- For Cypress CYUSB3KIT-003 "SuperSpeed Explorer Kit" (\$78)
- The board does not count as "Open Source HW" though but someone could design one.
- It's USB 3.0 !
- Interesting project anyway: <https://github.com/zeldin/fx3lafw>

Why this project?

Fast devices: closed source

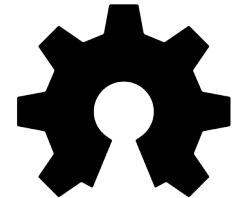
Open source devices: **cheap** and **slow**.

What about a fast, not so expensive, open source solution?

Target specifications

1/ Open source

- Hardware: design & production files
- PC Software: sigrok/PulseView
- Firmware: custom, powering on-board MCU
- FPGA Gateware: HDL sources, Migen/LiteX based
- Tools: Kicad, gcc, NextPNR, Yosys
- Licenses: CERN-OHL-W v2 and LGPL v2.1



open source
hardware

Target specifications

2/ **F A S T**

- USB 3.0 SuperSpeed (5 Gbps)
 - 100 Msps @ 16 probes
 - 200 Msps @ 8 probes
 - 400 Msps @ 4 probes

Target specifications

- 3/ Real-time streaming**
 - Capture very **long** sessions

Target specifications

4/ **Extensible**

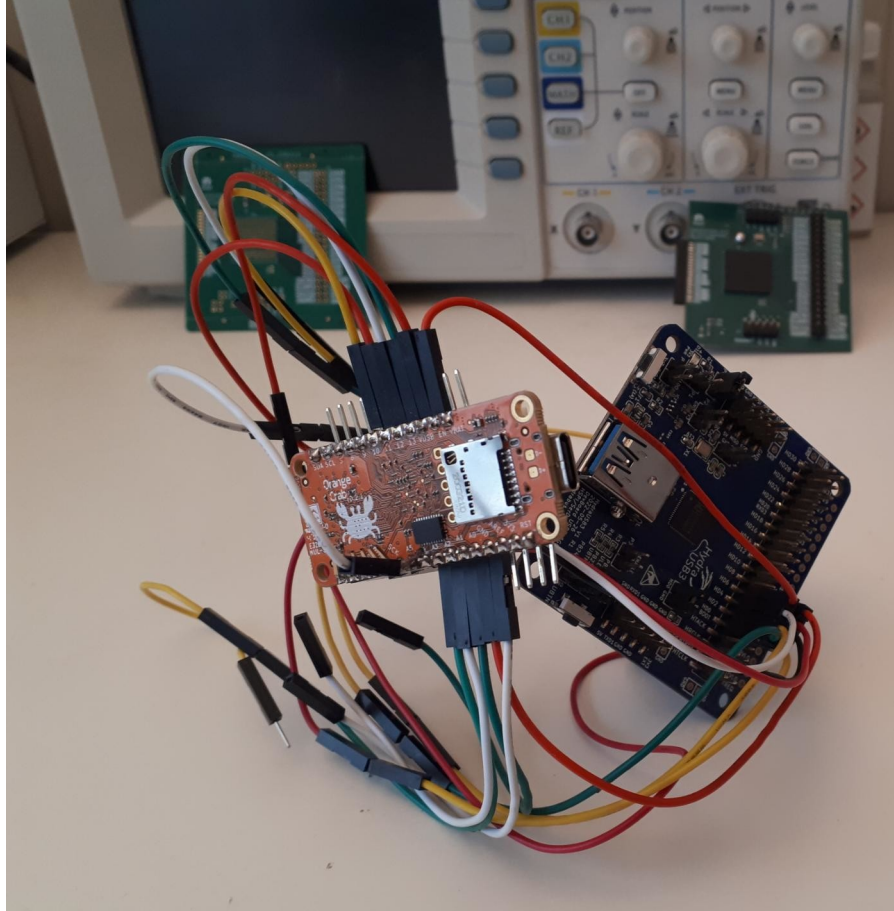
- FPGA based, with modularity in mind (dataflow/pipeline paradigm)
- Easy to learn/read/modify language: Migen (Python HDL)
- Reusing known SoC components: LiteX, Litescope
- Simple architecture (heavily based on litescope)

What has been done so far?

What has been done so far?

1st prototype:

- **OrangeCrab**
FPGA board
- **HydraUSB3**
mcu board
- **Lots of messy**
Jump wires.

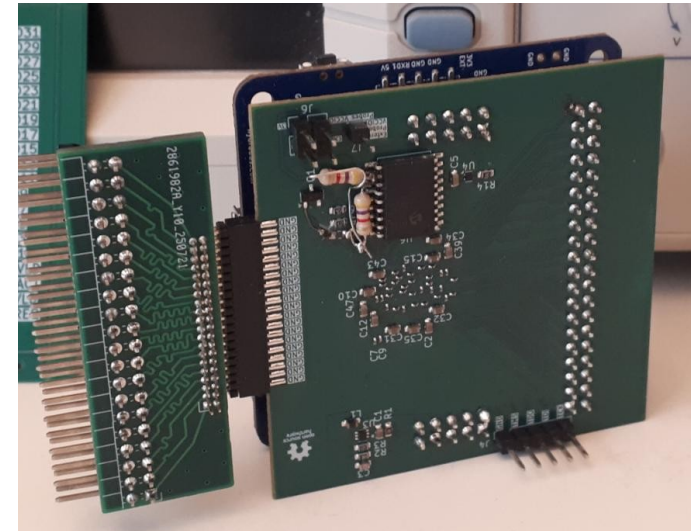
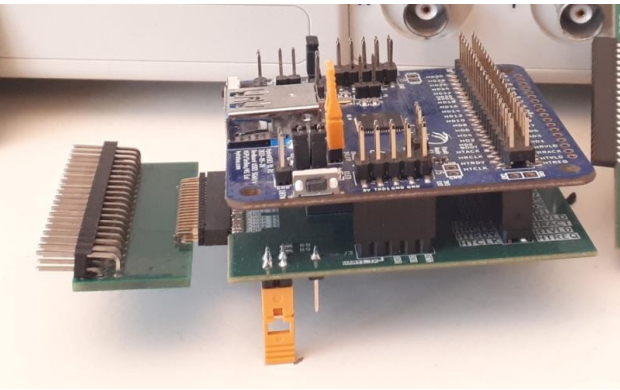
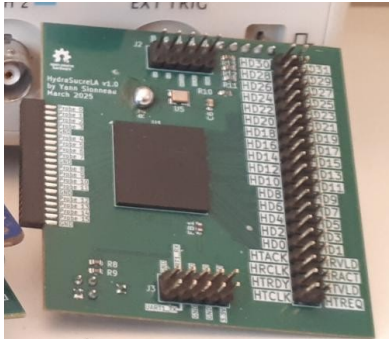


Was able to
capture samples
**@ 4 Msps on 4
probes**

What has been done so far?

2nd prototype:

- HydraUSB3
- Custom FPGA board:
HydraSucréLA
- No more messy wires!



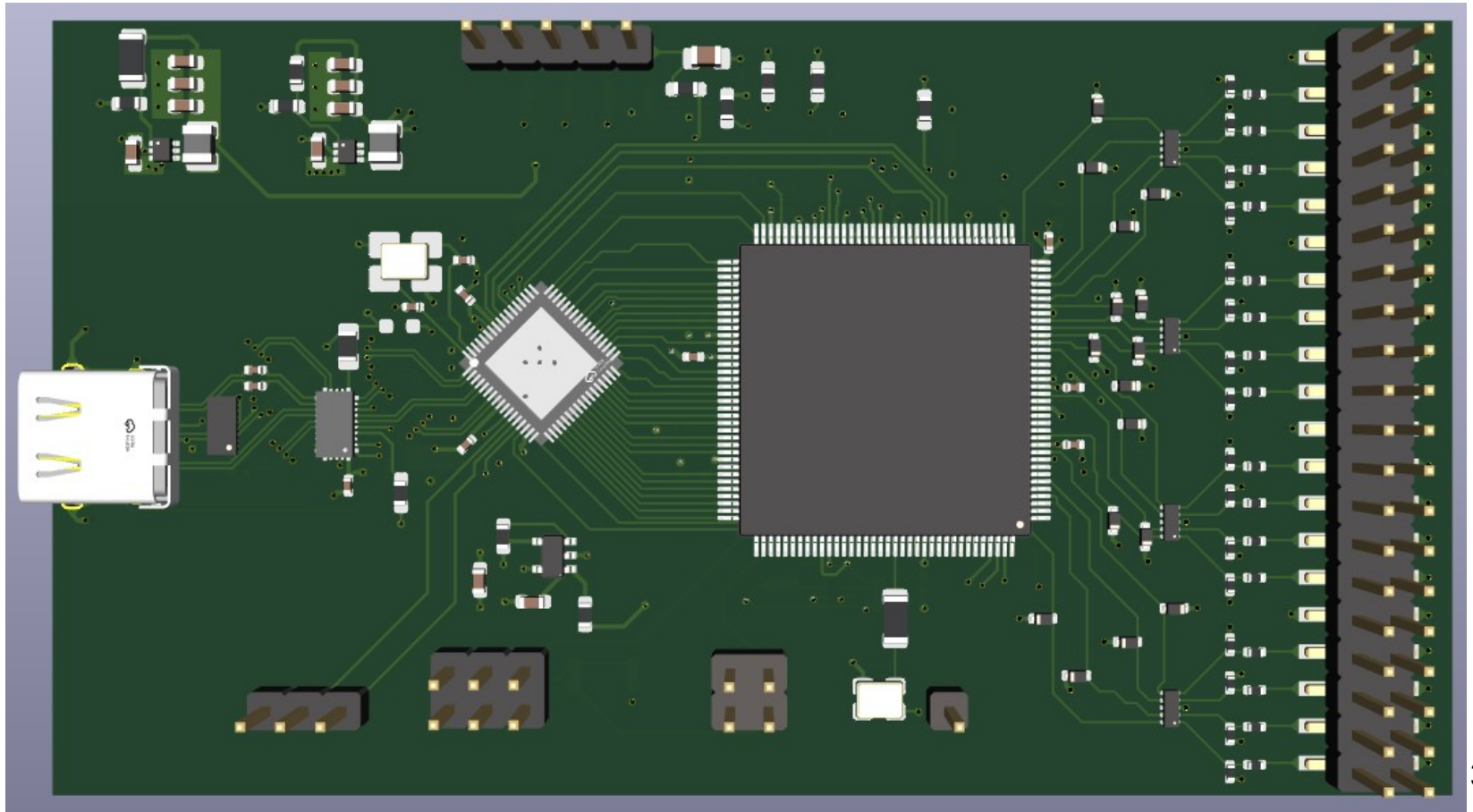
What has been done so far?

3rd prototype:
PCB received!
Bring-up barely started

What has been done so far?

3rd prototype:

- Everything on 1 single board: FPGA + MCU

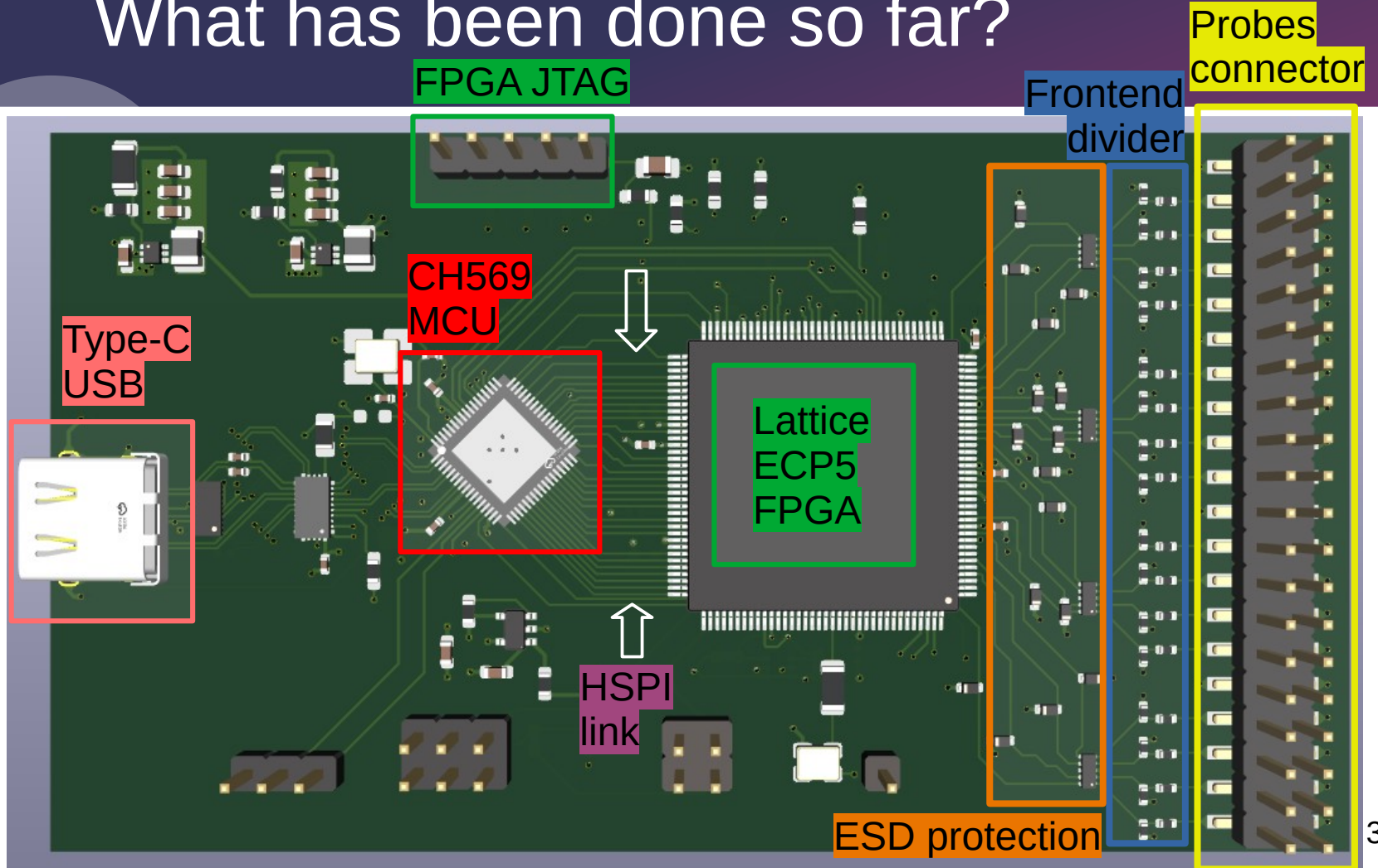


Top view
=>

What has been done so far?

3rd prototype:

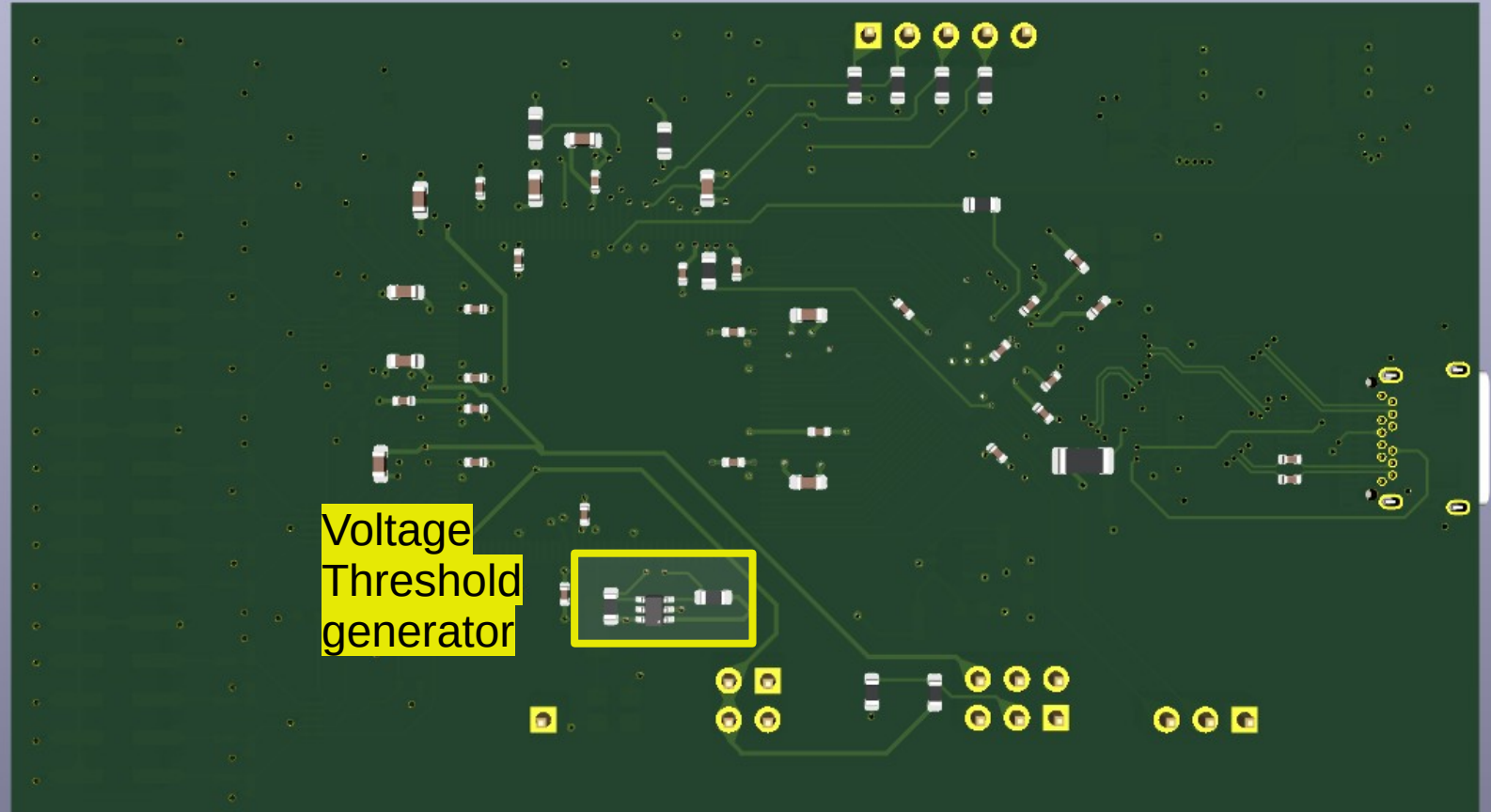
- Everything on 1 single board: FPGA + MCU



What has been done so far?

3rd prototype:

- Dynamically selectable sampling voltage threshold

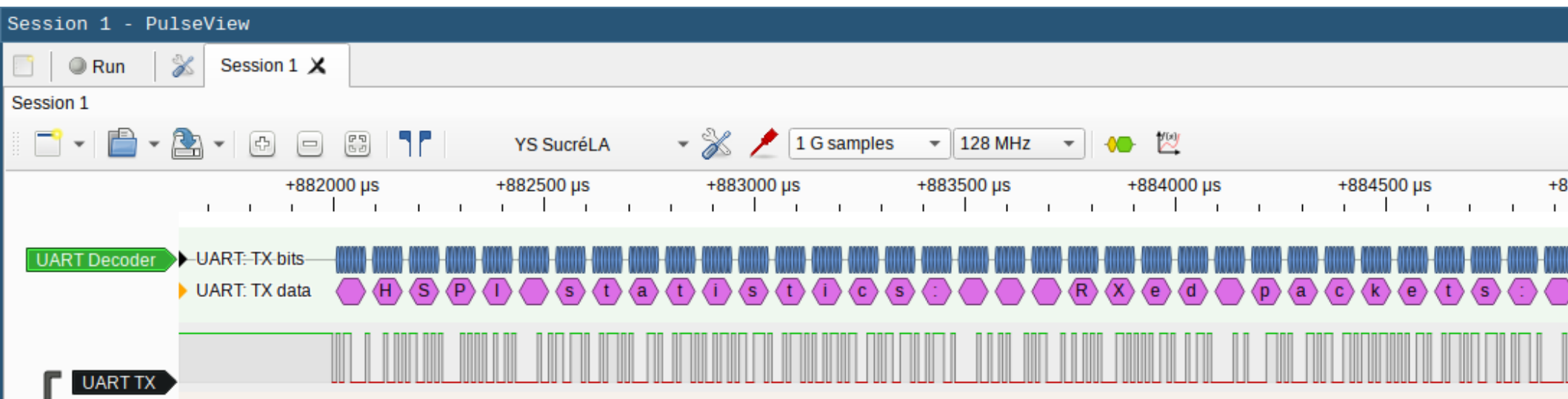


Bottom view

=>

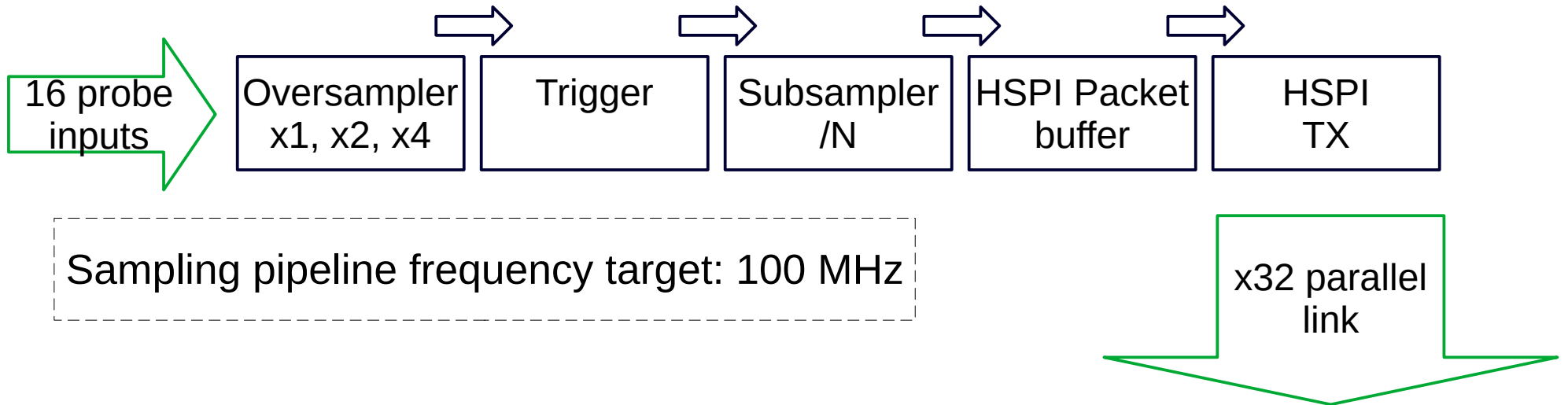
What has been done so far?

sigrok/PulseView support



What has been done so far?

The FPGA sampling pipeline

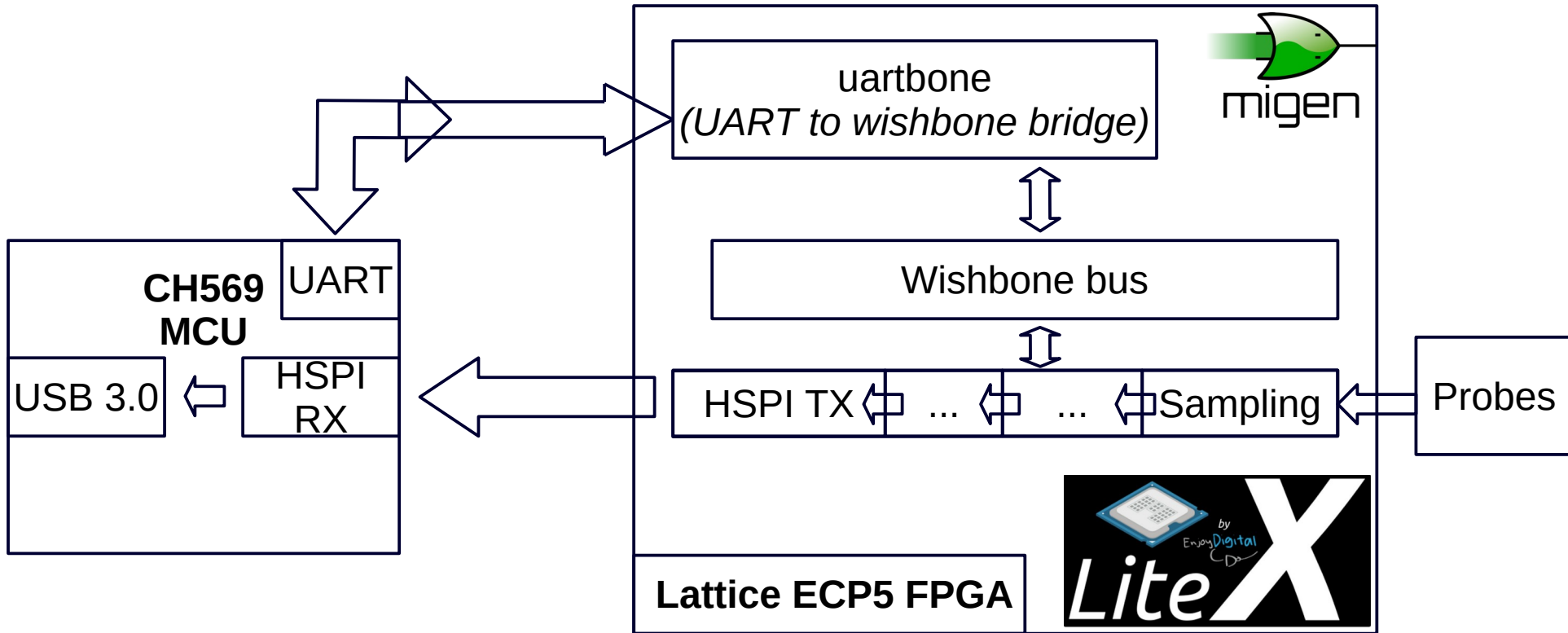


What has been done so far?

The USB 3.0 MCU firmware

- Get HSPI frames from FPGA
- Send them over USB 3.0 to Host PC
- USB-to-UART uartbone bridge to send wishbone read/write to FPGA SoC.
- USB programmer for the FPGA
- UART debug logs

Summary



What's next?

- 3rd prototype bring-up
- Improve libsigrok driver
- Improve documentation
- Integrate selectable voltage threshold feature
- Make HSPI x32 work
- Program FPGA over USB link
- Add RLE (run-length encoding) support
- Write a libscopehal/ngscopeclient driver
- Remove the MCU and do USB 3.0 with the FPGA?

Thank you!

Thank you!

Big up to **dok, jon, bvernoux** and the **#sigrok**
IRC channel on Libera :-)

Bon appétit !

“Bon appétit !”

<https://gitlab.com/yannسیونneau/SucreLA/>
yann [at] sionneau [dot] net